SIEMENS

Microcontrollers

Data Catalog

Contents

SIEMENS

Microcomputer Components

Microcontrollers

Data Catalog 1990

Note: Signals signified by a "# " are negated signals ($\overline{WR}$ = WR#)

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SAB 8088	8-bit Microprocessor (5 MHz, 8 MHz, 10 MHz)
SAB 80186	High-Integration 16-bit Microprocessor (8 MHz, 10 MHz)
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SAB 80286	High-Performance 16-bit Microprocessor with Memory Management and Protection (8 MHz, 10 MHz or 12.5 MHz)

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HYB 51100B -60/-70/-80 HYB 51100BL-60/-70	1M × 1-bit Dynamic RAM
HYB 514100 -80/-10	4M × 1-bit Dynamic RAM
HYB 514400 -80/-10	1M × 4-bit Dynamic RAM

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HYM 91000S -60/-70 HYM 91000L-60/-70/-80 HYM 91000SL-60/-70 HYM 91000LL-60/-70/-80	1M × 9-bit Dynamic RAM Modul
HYM 94000S -80/-10	4M × 9-bit Dynamic RAM Modul
HYM 362500S-80	256K × 36-bit Dynamic RAM Module
HYM 365120S-80	512K × 36-bit Dynamic RAM Module
HYM 361020S-80/-10	1M × 36-bit Dynamic RAM Module
HYM 362020S-80/-10	2M × 36-bit Dynamic RAM Module

General Information

General Information

Type designation code for ICs

IC type designations are based on the European Pro Electron system. The code system is explained in the Pro Electron brochure D 15, edition 1985, available at:

Pro Electron, Avenue Louise, 430 (B. 12)
B-1060 Brussels, Belgium

Mounting instructions

Plastic Package

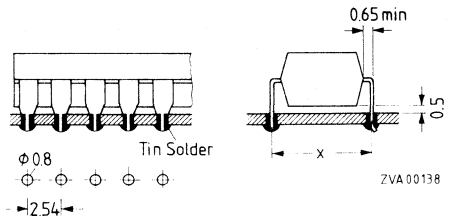
The 90° pins fit into holes with a diameter of 0.7 to 0.9 mm, spaced 2.54 mm apart. See spacing x in figure 1.

The bottom of the package will not touch the PC board after insertion because the pins have shoulders just below the package **(see figure 1)**.

After insertion of the package into the PC board it is advisable to bend the ends of two pins at an angle of approx. 30° to the board so that the package does not have to be pressed down during soldering. Plastic packages are soldered on that side of the PCB facing away from the package.

The maximum permissible soldering temperature is 350 °C (max. 3 s) for hand soldering and 260 °C (max. 10 s) for dip soldering and wave soldering.

Figure 1



Dimensions in mm

Plastic packages (SO and PLCC) for surface mounting (SMD)

Iron soldering:	soldering temperature 350 °C for max. 3 s; minimum distance between package and soldering point 1.5 mm package temperature max. 150 °C; no mechanical stress on the pins
Vapor phase soldering:	soldering temperature 215 °C, max. soldering time 40 s
Wave soldering: (pins and package are dipped into the tin bath)	soldering temperature 260 °C, max. soldering time 8 s

Storage, pretreatment before processing

The components are to be stored in a dry environment. When solder methods causing solder heat shock stresses are used (reflow soldering where the component is dipped into the solder bath, vapor-phase soldering) it is recommendable to subject IC's in plastic packages to a 24-hour drying phase at 125 °C.

Other points to note

Ensure that no current is able to flow between the solder bath or soldering iron and the PCB. It is advisable to ground the pins that are to be soldered as well as the solder bath or soldering iron.

When the pins are being prepared and inserted in a PCB, circuits should be protected against static charging. Under no circumstances should the components be removed or inserted while the operating voltage is switched on.

The increase in chip temperature during the soldering process results in a temporary increase in electrostatic sensitivity of integrated circuits. Special precautions should therefore be taken against line transients, e.g. through the switching of inductances on magnetic chutes, etc.

Processing guidelines for ICs

Integrated circuits (ICs) are **e**lectro**s**tatic-**s**ensitive (**ESS**) devices. The requirement for greater packing density has led to increasingly small structures on semiconductor chips with the result that today every IC, whether bipolar, MOS, or CMOS, has to be protected against electrostatics.

MOS and CMOS devices generally have integrated protective circuits and it is hardly possible any more for them to be destroyed by purely static electricity. On the other hand, there is acute danger from **e**lectro**s**tatic **d**ischarges (**ESD**).

Of the multiple of possible sources of discharge, charged devices should be mentioned in addition to charged persons. With low-resistive discharges it is possible for peak power amounting to kilowatts to be produced.

For the protection of devices the following principles should be observed:

a) Reduction of charging voltage, below 200 V if possible.
Means which are effective here are an increase in relative humidity to ≥ 60 % and the replacement of highly charging plastics by antistatic materials.

b) With every king of contact with the device pins a charge equalization is to be expected. This should always be highly resistive (ideally $R = 10^6$ to $10^8\ \Omega$).

All in all this means that ICs call for special handling, because uncontrolled charges, voltages from ungrounded equipment or persons, surge voltage spikes and similar influences can destroy a device. Even if devices have protective circuits (e.g. protective diodes) on their inputs, the following guidelines for their handling should nevertheless be observed.

Identification

The packing of ESS devices is provided with the following label by the manufacturer:

Scope

The guidelines apply to the storage, transport, testing, and processing of all kinds of ICs, equipped and soldered circuit boards that comprise such components.

Handling of devices

1. ICs must be left in their containers until they are processed.
2. ICs may only be handled at specially equipped work stations. These stations must have work surfaces covered with a conductive material of the order of 10^6 to $10^9\ \Omega$/cm.
3. With humidity of > 50 % a coat of pure cotton is sufficient. In the case of chargeable synthetic fibers the clothing should be worn close-fitting. The wrist strap must be worn snugly on the skin and be grounded across a resistor of 50 to 100 Ω.
4. If conductive floors, $R = 5 \times 10^4$ to $10^7\ \Omega$ are provided, further protection can be achieved by using so-called MOS chairs and shoes with a conductive sole ($R \approx 10^5$ to $10^7\ \Omega$).
5. All transport containers for ESS devices and assembled circuit boards must first be brought to the same potential by being placed on the work surface or touched by the operator before the individual devices may be handled. The potential equalization should be across a resistor of 10^6 to $10^8\ \Omega$.
6. When loading machines and production devices it should be noted that the devices come out of the transport magazine charged and can be damaged if they touch metal, e.g. machine parts.

Example 1) Conductive (black) tubes.
The devices may be destroyed in the tube by charged persons or come out of the tube charged if this in emptied by a charged person.
Conductive tubes may only be handled at ESS work stations (high-resistance work-station and person grounding).

Example 2) Anti-static (transparent) tubes.
The devices cannot be destroyed by charged persons in the tube (there may be a rare exception in the case of custom ICs with unprotected gate pins).
The devices can be endangered as in 1) when the tube is emptied if the latter, especially at low humidity, is no longer sufficiently anti-static after a long period of storage (> 1 year).

In both cases damage can be avoided by discharging the devices across a grounded adapter of high-resistance material ($\approx 10^6$ to $10^8\ \Omega$/cm) between the tube and the machine.

The use of metal tubes – especially of anodized aluminum – is not advisable because of the danger of low-resistance device discharge.

Storage

ESS devices should only be stored in identified locations provided for the purpose. During storage the devices should remain in the packing in which they are supplied. Thestorage temperature should not exceed 60 °C.

Transport

ESS devices in approved packing tubes should only be transported in suitable containers of conductive or longterm anti-static-treated plastic or possibly unvarnished wood. Containers of high-charging plastic or very low-resistance materials are likewise unsuitable.

Transfer cars and their rollers should exhibit adequate electrical conductivity ($R < 10^6\ \Omega$). Sliding contacts and grounding chains will not reliably eliminate charges.

Incoming inspection

In incoming inspection the above guidelines should be observed. Otherwise any right for refund or replacement if devices fail inspection may be lost.

Material and mounting

1. The drive belts of machines used for the processing of the devices, in as much as they come into contact with them (e.g. bending and cutting machines, conveyor belts), should be treated with anti-static spray (e.g. anti-static spray 100 from Kontaktchemie). It is better, however, to avoid the contact completely.
2. If ESS devices have to be soldered or desoldered manually, soldering irons with thyristor control cannot be used. Siemens EMI-suppression capacitors of the type B 81711-B31 ... -B36 have propen very effective against line transients.
3. Circuit boards fitted and soldered with ESS devices are always to be considered as endangered.

Electrical tests

1. The devices should be processed with observation of these guidelines. Before assembled and soldered circuit boards are tested, remove any shorting ring.
2. Test sockets must not be conducting any voltage when individual devices or assembled circuit boards and inserted or withdrawn, unless works' specifications state otherwise. Ensure that the test devices do not produce any voltage spikes, either when being turned on and off in normal operation or if the power fuse blows or other fuses respond.
3. Signal voltages may only be applied to the inputs of ICs when or after the supply voltage is turned on. They must be disconnected before or when the supply voltage is turned off.
4. Observe any notes and instructions in the respective data books.

Packing of assembled PC boards or flatpack units

The packing material should exhibit low volume conductivity:
$10^5\ \Omega/cm < \rho < 10^{10}\ \Omega/cm$.

In most cases - especially with humidity of > 40 % - this requirement is fulfilled using simple currugated board. Better protection is obtained with bags of conductive polyethylene foam (e.g. RCAS 1200 from Richmond of Redlands, California).

It must always be ensured that boards do not touch.

In special cases it may be necessary to provide potection against strong electric fields, such as can be generated by conveyor belts for example. For this purpose a sheath of aluminum foil is recommended, although direct contact between the film and the PCB must be avoided. Cardboard boxes with an aluminum-foil lining, such as those used for shipping of our devices, are available from Laber of Munich.

Ultrasonic cleaning of ICs

In incoming inspection the above guidelines should be observed. Otherwise any right for refund or replacement if devices fail inspection may be lost.

The following recommendation applies to plastic packages. For cavity packages (metal and also ceramic) separate regulations have to be observed.

Freon and isopropyl alcohol (trade name: propanol) can be used as solvents. These solvents can also be used for plastic packages because they do not eat into the plastic material.

An ultrasonic bath in double halfwave operation is advisable because of the low component stress.

The ultrasonic limits are as follows:

sound frequency	f > 40 kHz
exposure	t > 2 min
alternating sound pressure	p > 0.29 bar
sound power	N > 0.5 W/cm²/liter

Data classification

Maximum ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics will apply at T_A = 25 °C and for the given supply voltage.

Operating range

In the operating range the functions given in the circuit description will be fulfilled.

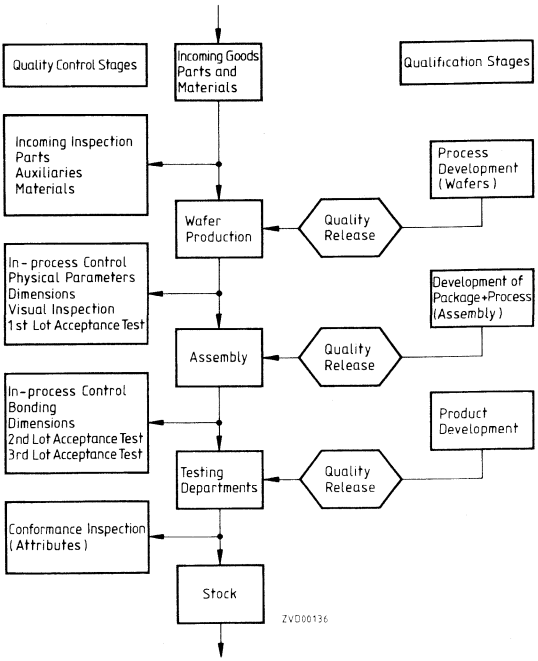
Quality assurance system

The high quality and reliability of integrated circuits from Siemens is the result of a carefully arranged production which is systematically checked and controlled at each production stage.

The procedures are subject to a quality assurance system; full details are given in the brochure "Siemens Quality Assurance System - Integrated Circuits" (SQS-IC).

Figure 4 shows the most important stages of the "SQS-IC". A quality assurance (QA) department which is independent of production and development, is responsible for the selected control measures, acceptance procedures, and information feedback loops. This department has state-of-the-art test and measuring equipment at its disposal, works according to approved methods of statistical quality control, and is provided with facilities for accelerated life and environmental tests used for both qualification and routine monitoring tests.

Figure 4



The latest methods and equipment for preparation and analysis are employed to achieve continuity of quality and reliability.

Conformance

Each integrated circuit is subjected to a final test at the end of the production process. These tests are carried out by computer-controlled, automatic test systems because hundreds of thousands of operating conditions as well as a large number of static and dynamic parameters have to be considered. Moreover, the test systems are extremely reliable and reproducible. The quality assurance department carries out a final check in the form of a lot-by-lot sampling inspection to additionally ensure this minimum percent defectives as well as the acceptable quality level (AQL). Sampling inspection is performed in accordance with the inspection plans of DIN 40080, as well as of the identical MIL-STD-105 or IEC 410.

The table shows the results of such sampling inspections performed with hundreds of thousands of ICs in 1985. These results correspond to the average outgoing quality (AOQ), and are specified as defectives per million (DPM).

	Inoperatives AOQ (DPM)	**Sum of electrical defectives AOQ (DPM)**	**Sum of mechanical defectives AOQ (DPM)**
SSI/MSI ≤ 1000 gate functions	40	200	100
LSI/MSI ≤ 1000 gate functions	120	400	200

Reliability

Measures taken during development

The reliability of ICs is already considerably influenced at the development stage. Siemens has, therefore, fixed certain design standards for the development of circuit and layout, specifying e.g. minimum width and spacing of conductive layers on a chip, dimensions and electrical parameters of protective circuits for electrostatic charge, etc. An examination with the aid of carefully arranged programs operated on large-scale computers, guarantees the immediate identification and elimination of unintentional violations of these design standards.

In-process control during production

The manufacturing of integrated circuits comprises several hundred production steps. As each step is to be executed with utmost accuracy, the in-process control is of outstanding importance. Some processes require more than a hundred different test measures. The tests have been arranged such that the individual process steps can be reproduced continuously.

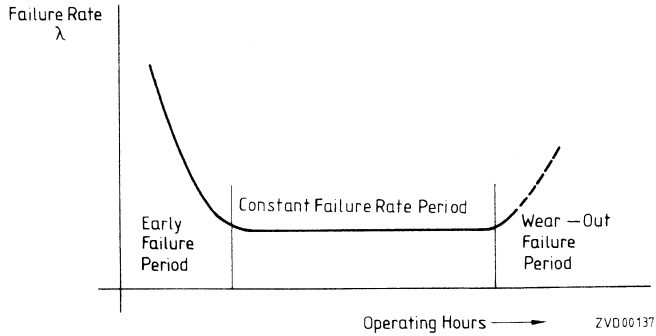
The decreasing failure rates reflect the never ending effort in this direction; they have been reduced considerably despite an immense rise in the IC's complexity.

So in 1985 the typical random failure rates estimated for accelerated life tests with almost 2 million ICs of all complexities are found to be around 80 fit.

Reliability monitoring

The general course of the ICsfailurerateversustimeis'shown by a so-called "bathtub" curve (**figure 5**). The failure rate has its peak during the first few operating hours (early failure period). After the early failure period has decayed, the "constant" failure rate period starts during which the failures may occur at an approximately uniform rate. This period ends with a repeated rise of the curve during the wear-out failure period. For ICs, however, the latter period usually lies far beyond the service life specified for the individual equipment.

Figure 5



Reliability tests for ICs are usually destructive examinations. They are, therefore, carried out with samples. Most failure mechanisms can be accelerated by means of higher temperatures. Due to the temperature dependence of the failure mechanisms, it is possible to simulate future operational behavior within a short time by applying high temperatures; this is called life test.

The acceleration factor B for the life test can be obtained from the Arrhenius equation

$$B = \exp \frac{E_A}{k}\left[\frac{1}{T_1} - \frac{1}{T_2}\right]$$

where T_2 is the temperature at which the life test is performed, T_1 is the assumed operating temperature, and k is the Boltzmann constant.

Important for factor B is the activation energy E_A. It lies between 0.3 and 1.3 eV and differs considerably for individual failure mechanisms.

For all Siemens ICs, the reliability data from life tests is converted to an operating temperature of T_A = 40 °C, assuming an average activation energy of 0.4 eV. The acceleration factor for life tests at 125 °C is thus 24, compared with operational behavior. This method considers also failure mechanisms with low activation energy, i.e. which are only slightly accelerated by the temperature effect.

Various reliability tests are periodically performed with IC types that are representative of a certain production line - this is described in the brochure "SQS-IC". Such tests are e.g. humidity test at 85 °C and 85 % relative humidity, pressure cooker test, as well as life tests up to 1000 hours and more. Test results are available in the form of summary reports.

Summary of Types (incl. ordering codes)

Summary of Types

Type	Ordering Code	Package	Description	Page
8-Bit Single-Chip Microcontrollers				
SAB 8031A-10-P-T40/110	Q67120-C232	P-DIP-40	without ROM ext. Temp.: – 40 to + 110 °C	309
SAB 8031A-12-P-T40/85	Q67120-C230	P-DIP-40	without ROM ext. Temp.: – 40 to + 85 °C	309
SAB 8031A-16-N	Q67120-C349	PL-CC-44	without ROM	285
SAB 8031A-16-P	Q67120-C347	P-DIP-40	without ROM	285
SAB 8031A-N	Q67120-C271	PL-CC-44	without ROM	285
SAB 8031A-P	Q67120-C183	P-DIP-40	without ROM	285
SAB 8032A-N	Q67120-C264	PL-CC-44	without ROM	329
SAB 8032A-N-T40/85	Q67120-C367	PL-CC-44	without ROM ext. Temp.: – 40 to + 85 °C	351
SAB 8032A-P	Q67120-C196	P-DIP-40	without ROM	329
SAB 8032A-P-T40/100	Q67120-C239	P-DIP-40	without ROM ext. Temp.: – 40 to + 100 °C	351
SAB 8032A-P-T40/85	Q67120-C235	P-DIP-40	without ROM ext. Temp.: – 40 to + 85 °C	351
SAB 8032B-16-N	Q67120-C425	PL-CC-44	without ROM	375
SAB 8032B-16-P	Q67120-C421	P-DIP-40	without ROM	375
SAB 8032B-20-N	Q67120-C472	PL-CC-44	without ROM	375
SAB 8032B-20-P	Q67120-C471	P-DIP-40	without ROM	375
SAB 8032B-N	Q67120-C423	PL-CC-44	without ROM	375
SAB 8032B-P	Q67120-C419	P-DIP-40	without ROM	375
SAB 8035L-P-T40/85	Q67120-C140	P-DIP-40	without ROM ext. Temp.: – 40 to + 85 °C	39

Summary of Types (cont'd)

Type	Ordering Code	Package	Description	Page
8-Bit Single-Chip Microcontrollers (cont'd)				
SAB 8048-P-T40/110	Q67120-C162	P-DIP-40	1K × 8 ROM ext. Temp.: – 40 to + 110 °C	39
SAB 8048-P-T40/85	Q67120-C133	P-DIP-40	1K × 8 ROM ext. Temp.: – 40 to + 85 °C	39
SAB 80512-N	Q67120-C336	PL-CC-68	4K × 8 ROM	59
SAB 80512-N-T40/85-N	Q67120-C353	PL-CC-68	4K × 8 ROM ext. Temp.: – 40 to + 85 °C	59
SAB 80512K-A	Q67120-C333	C-PGA-88	ROM-less Version	57
SAB 80513-16-N	Q67120-C443	PL-CC-44	16K × 8 ROM, 16 MHz	85
SAB 80513-16-P	Q67120-C441	P-DIP-40	16K × 8 ROM, 16 MHz	85
SAB 80513-16-P-T3	Q67120-C506	P-DIP-40	16K × 8 ROM, 16 MHz ext.Temp.: – 40 to +85 °C	85
SAB 80513-N	Q67120-C384	PL-CC-44	16K × 8 ROM	85
SAB 80513-P	Q67120-C383	P-DIP-40	16K × 8 ROM	85
SAB 80515-N	Q67120-C211	PL-CC-68	8K × 8 ROM	109
SAB 80515-N-T40/110	Q67120-C316	PL-CC-68	8K × 8 ROM, 12 MHz ext. Temp.: – 40 to + 110 °C	145
SAB 80515-N-T40/85	Q67120-C210	PL-CC-68	8K × 8 ROM, 12 MHz ext. Temp.: – 40 to + 85 °C	145
SAB 80515K-A	Q67120-C267	C-PGA-88	ROM-less Version	179

Summary of Types (cont'd)

Type	Ordering Code	Package	Description	Page
8-Bit Single-Chip Microcontrollers (cont'd)				
SAB 8051A-10-P-T40/110	Q67120-C231	P-DIP-40	4K × 8 ROM ext. Temp.: – 40 to + 110 °C	309
SAB 8051A-12-P-T40/85	Q67120-C233	P-DIP-40	4K × 8 ROM ext. Temp.: – 40 to + 85 °C	309
SAB 8051A-16-N	Q67120-C348	PL-CC-44	4K × 8 ROM	285
SAB 8051A-16-P	Q67120-C346	P-DIP-40	4K × 8 ROM	285
SAB 8051A-N	Q67120-C224	PL-CC-44	4K × 8 ROM	285
SAB 8051A-P	Q67120-C186	P-DIP-40	4K × 8 ROM	285
SAB 8052A-N	Q67120-C263	PL-CC-44	8K × 8 ROM	329
SAB 8052A-N-T40/85	Q67120-C368	PL-CC-44	8K × 8 ROM ext. Temp.: – 40 to + 85 °C	351
SAB 8052A-P	Q67120-C195	P-DIP-40	8K × 8 ROM	329
SAB 8052A-P-T40/100	Q67120-C248	P-DIP-40	8K × 8 ROM ext. Temp.: – 40 to + 100 °C	351
SAB 8052A-P-T40/85	Q67120-C247	P-DIP-40	8K × 8 ROM ext. Temp.: – 40 to + 85 °C	351
SAB 8052B-16-N	Q67120-C426	PL-CC-44	8K × 8 ROM, 16 MHz	375
SAB 8052B-16-P	Q67120-C422	P-DIP-40	8K × 8 ROM, 16 MHz	375
SAB 8052B-N	Q67120-C424	PL-CC-44	8K × 8 ROM, 12 MHz	375
SAB 8052B-P	Q67120-C420	P-DIP-40	8K × 8 ROM	375
SAB 80532-N	Q67120-C337	PL-CC-68	without ROM	59
SAB 80532-T40/85	Q67120-C354	PL-CC-68	without ROM ext. Temp.: – 40 to + 85 °C	59

Summary of Types (cont'd)

Type	Ordering Code	Package	Description	Page
8-Bit Single-Chip Microcontrollers (cont'd)				
SAB 80535-N	Q67120-C241	PL-CC-68	without ROM	109
SAB 80535-N-T40/110	Q67120-C313	PL-CC-68	without ROM ext.Temp.: – 40 to +110°C	145
SAB 80535-N-T40/85	Q67120-C240	PL-CC-68	without ROM ext.Temp.: – 40 to + 85 °C	145
SAB 80C32-16-N	Q67120-C502	PL-CC-44	without ROM, 16 MHz	399
SAB 80C32-16-P	Q67120-C500	P-DIP-40	without ROM, 16 MHz	399
SAB 80C32-16-P-T40/85	Q67120-C527	P-DIP-40	without ROM, 16 MHz ext.Temp.: – 40 to + 85 °C	399
SAB 80C32-N	Q67120-C395	PL-CC-44	without ROM	399
SAB 80C32-N-T40/110	Q67120-C548	PL-CC-44	without ROM, 12 MHz ext.Temp.: – 40 to +110°C	399
SAB 80C32-N-T40/85	Q67120-C540	PL-CC-44	without ROM, 12 MHz ext.Temp.: – 40 to + 85 °C	399
SAB 80C32-P	Q67120-C378	P-DIP-40	without ROM	399
SAB 80C32-P-T40/110	Q67120-C547	P-DIP-40	without ROM, 12 MHz ext.Temp.: – 40 to +110°C	399
SAB 80C32-P-T40/85	Q67120-C520	P-DIP-40	without ROM, 12 MHz ext.Temp.: – 40 to + 85 °C	399
SAB 80C515-16-N	Q67120-C492	PL-CC-68	8K × 8 ROM, 16 MHz	181
SAB 80C515-16-N-T40/85	Q67120-C561	PL-CC-68	8K × 8 ROM, 16 MHz ext.Temp.: – 40 to + 85 °C	181
SAB 80C515-N	Q67120-C297	PL-CC-68	CMOS, 8K × 8 ROM, 12 MHz	181
SAB 80C515-N-T40/110	Q67120-C391	PL-CC-68	8K × 8 ROM, 12 MHz ext.Temp.: – 40 to +110°C	181
SAB 80C515-N-T40/85	Q67120-C388	PL-CC-68	8K × 8 ROM, 12 MHz ext.Temp.: – 40 to + 85 °C	181

Summary of Types (cont'd)

Type	Ordering Code	Package	Description	Page
8-Bit Single-Chip Microcontrollers (cont'd)				
SAB 80C517-16-N	Q67120-C723	PL-CC-84	CMOS 8K × 8 ROM,16 MHz	231
SAB 80C517-16-N-T40/110	Q67120-C726	PL-CC-84	CMOS 8K × 8 ROM,16 MHz ext.Temp.: – 40 to +110 °C	231
SAB 80C517-16-N-T40/85	Q67120-C724	PL-CC-84	CMOS 8K × 8 ROM,12 MHz	231
SAB 80C517-N	Q67120-C397	PL-CC-84	CMOS 8K × 8 ROM,12 MHz	231
SAB 80C517-N-T40/110	Q67120-C721	PL-CC-84	CMOS 8K × 8 ROM,12 MHz ext.Temp.: – 40 to +110 °C	231
SAB 80C517-N-T40/85	Q67120-C483	PL-CC-84	CMOS 8K × 8 ROM,12 MHz ext.Temp.: – 40 to + 85 °C	231
SAB 80C52-16-N	Q67120-C503	PL-CC-44	8K × 8 ROM, 16 MHz	399
SAB 80C52-16-N-T40/85	Q67120-C528	PL-CC-44	8K × 8 ROM, 16 MHz ext. Temp.: – 40 to + 85 °C	399
SAB 80C52-16-P	Q67120-C501	P-DIP-40	8K × 8 ROM, 16 MHz	399
SAB 80C52-16-P-T40/85	Q67120-C563	P-DIP-40	8K × 8 ROM, 16 MHz ext. Temp.: – 40 to + 85 °C	399
SAB 80C52-N	Q67120-C396	PL-CC-44	8K × 8 ROM	399
SAB 80C52-N-T40/100	Q67120-C559	PL-CC-44	8K × 8 ROM, 12 MHz ext.Temp.: – 40 to +100 °C	399
SAB 80C52-N-T40/85	Q67120-C564	PL-CC-44	8K × 8 ROM, 12 MHz ext. Temp.: – 40 to + 85 °C	399
SAB 80C52-P	Q67120-C379	P-DIP-40	8K × 8 ROM	399
SAB 80C52-P-T40/100	Q67120-C558	P-DIP-40	8K × 8 ROM, 12 MHz ext.Temp.: – 40 to +100 °C	399
SAB 80C52-P-T40/85	Q67120-C521	P-DIP-40	8K × 8 ROM, 12 MHz ext.Temp.: – 40 to + 85 °C	399

Summary of Types (cont'd)

Type	Ordering Code	Package	Description	Page
8-Bit Single-Chip Microcontrollers (cont'd)				
SAB 80C535-16-N	Q67120-C509	PL-CC-68	without ROM, 16 MHz	181
SAB 80C535-16-N-T40/85	Q67120-C562	PL-CC-68	without ROM, 16 MHz ext.Temp.: – 40 to + 85 °C	181
SAB 80C535-N	Q67120-C508	PL-CC-68	without ROM	181
SAB 80C535-N-T40/110	Q67120-C538	PL-CC-68	without ROM, 12 MHz ext.Temp.: – 40 to +110 °C	181
SAB 80C535-N-T40/85	Q67120-C510	PL-CC-68	without ROM, 12 MHz ext.Temp.: – 40 to + 85 °C	181
SAB 80C537-16-N-T40/85	Q67120-C725	PL-CC-84	CMOS, without ROM, 16 MHz ext.Temp.: – 40 to + 85 °C	231
SAB 80C537-16-N	Q67120-C722	PL-CC-84	CMOS, without ROM, 16 MHz	231
SAB 80C537-16-N-T40/110	Q67120-C727	PL-CC-84	CMOS, without ROM, 16 MHz ext.Temp.: – 40 to +110 °C	231
SAB 80C537-S-T40/110	Q67120-C717	P-QFP-100	CMOS, without ROM, 12 MHz ext.Temp.: – 40 to +110 °C	231
SAB 80C537-N	Q67120-C452	PL-CC-84	CMOS, without ROM, 12 MHz	231
SAB 80C537-N-T40/110	Q67120-C571	PL-CC-84	CMOS, without ROM, 12 MHz ext.Temp.: – 40 to +110 °C	231
SAB 80C537-N-T40/85	Q67120-C484	PL-CC-84	CMOS, without ROM, 16 MHz ext.Temp.: – 40 to + 85 °C	231

Summary of Types (cont'd)

Type	Ordering Code	Package	Description	Page
8-Bit Single-Chip Microcontrollers (cont'd)				
SAB 83515-4-N	Q67120-C525	PL-CC-68	16K × 8 ROM	427
SAB 83515-4-N-T3	Q67120-C536	PL-CC-68	16K × 8 ROM, ext. Temp.: – 40 to + 85 °C	427
SAB 83515-4-N-T4	Q67120-C539	PL-CC-68	16K × 8 ROM, ext.Temp.: – 40 to +110 °C	427
SAB 8352-5-16-N	Q67120-C533	PL-CC-44	32K × 8 ROM, 16 MHz	85
SAB 8352-5-16-P	Q67120-C529	P-DIP-40	32K × 8 ROM, 16 MHz	85
SAB 8352-5-16-P-T3	Q67120-C531	P-DIP-40	32K × 8 ROM, 16 MHz ext. Temp.: 0 to + 70 °C	85
SAB 8352-5-N	Q67120-C524	PL-CC-44	32K × 8 ROM	85
SAB 8352-5-P	Q67120-C526	P-DIP-40	32K × 8 ROM	85
16-Bit Single-Chip Microcontrollers				
SAB 80C166-S	Q67120-C493	P-QFP-100	without ROM	465
SAB 83C166-3S	Q67120-C552	P-QFP-100	8K × 8 ROM	465

8-Bit Single-Chip Microcontrollers

8 Bit Single Chip Microcontroller

obsolescent Type

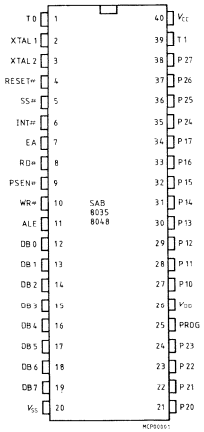
SAB 8035/8048

Extended Temperature Range: – 40 to + 85 °C
– 40 to + 110 °C

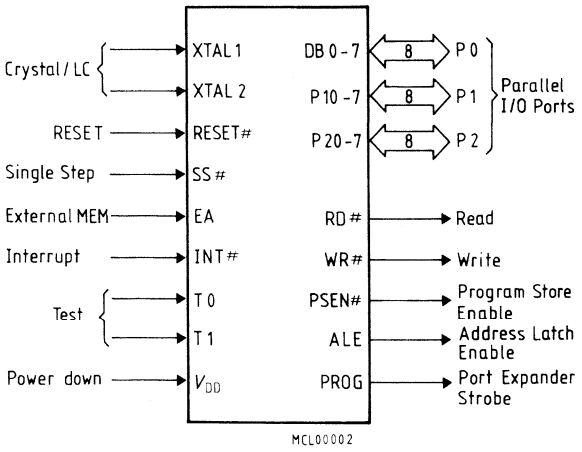
SAB 8048-P-T40/85	**Mask Programmable ROM**
SAB 8048-P-T40/110	**Mask Programmable ROM**
SAB 8035L-P-T40/85	**External ROM**

- 8-Bit CPU, ROM, RAM, I/O in Single Package
- 8-Bit Internal Timer/Event Counter
- Instructions 1 or 2 Cycles, 2.5 µs or 5.0 µs Cycle Time
- 96 Instructions: 70 % Single Byte
- Compatible with SAB 8080/8085 Peripherals
- 1K × 8 ROM
  64 × 8 RAM
  27 I/O Lines
- 2 Single Level Interrupts: Internal Timer/Counter and External
- Single 5 V Supply
- Power Down Mode: Standby Current for Internal RAM 15 mA

Pin Configuration



Logic Symbol



The SAB 8048/8035L are 8-Bit Single-Chip-Microcontroller implemented in + 5 Volts, depletion load, N channel, silicon gate Siemens MYMOS technology packaged in a 40 pin package. It is 100 % compatible with the industry standard 8048.

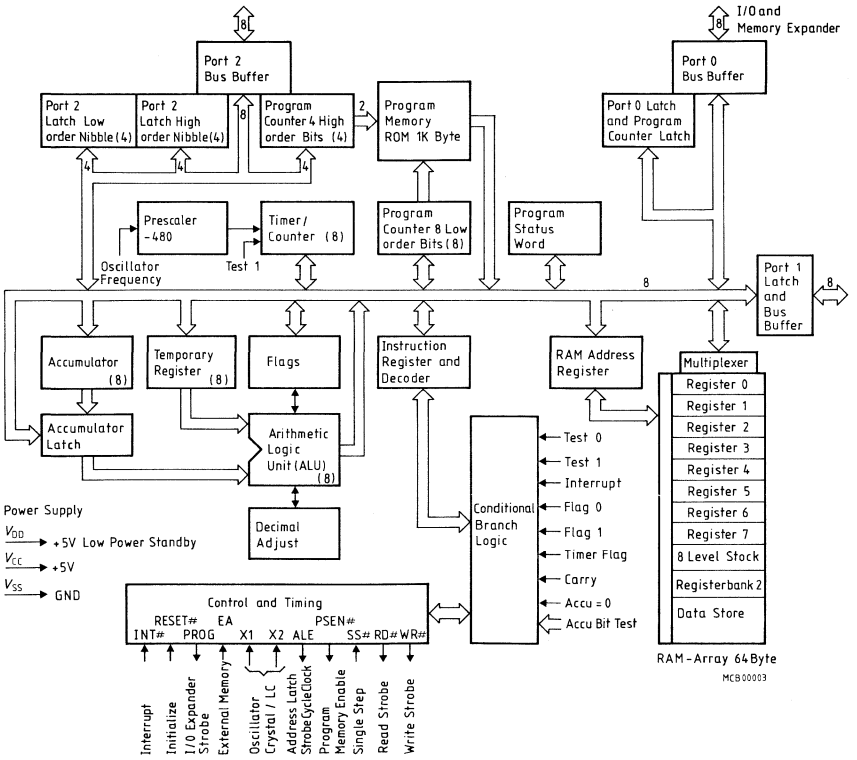
The SAB 8048 contains a 1K × 8 program memory, a 64 × 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the SAB 8048 can be expanded using standard memories and SAB 8080/8085 peripherals. The SAB 8035L is the equivalent of an SAB 8048 without program memory and can be used with external ROM and RAM.

These microcomputers are designed to be efficient controllers as well as arithmetic processors. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from a instruction set consisting mostly of single byte instructions and no instructions over 2 bytes in length.

Pin Description

Symbol	Pin No.	I/O	Function
T_0	1	I/O	Input pin testable using the conditional transfer instructions JT0 and JNT0. T_0 can be designated as a clock output using ENT0 CLK instruction
$XTAL_1$, $XTAL_2$	2, 3		Inputs for internal oscillator with crystal or external source (non TTL VIH)
$\overline{RESET}$	4	I	Input which is used to initialize the processor (Activ low). Also used during power down (non TTL VIH)
$\overline{SS}$	5	I	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction (active low)
$\overline{INT}$	6	I	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction (active low).
EA	7	I	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification (active high)
$\overline{RD}$	8	O	Output strobe activated during a BUS read. Can be used to enable data on the bus from an external device. Used as a read strobe to external data memory (active low)
$\overline{PSEN}$	9	O	Program store enable. This output occurs only during a fetch to external program memory (active low)
$\overline{WR}$	10	O	Output strobe during a bus write (active low). Used as a write strobe to external data memory
ALE	11	O	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory
$DB_0 - DB_7$	12-19	I/O	Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, RD, and WR
$P_{20} - P_{27}$	21-24 35-38	I/O	8-Bit quasi-bidirectional I/O-Port. P_{20}-P_{23} contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for SAB 8243
PROG	25	O	Output strobe for SAB 8243 I/O expander
$P_{10} - P_{17}$	27-34	I/O	8-Bit quasi-bidirectional I/O-Port.
T_1	39	I	Input pin testable using the JT1 and JTN1 instructions. Can be designated the timer/counter input using the STRT CNT instruction
V_{CC}	40		5 V Main power supply
V_{DD}	26		5 V Power Down Voltage
V_{SS}	20		GND potential

Block Diagram



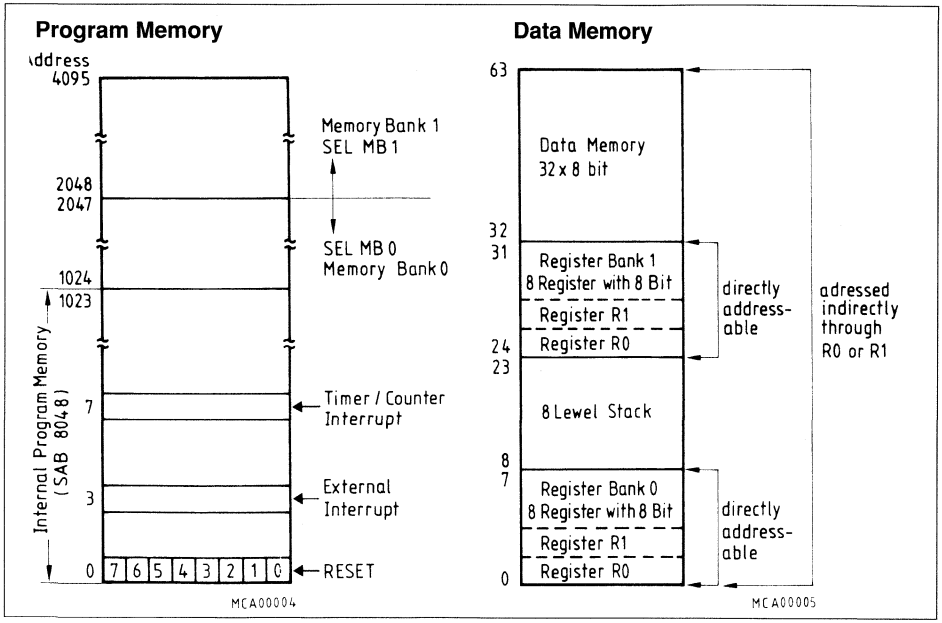
Functional Description

Program Memory

Program memory of SAB 8048 consists of 1024 words 8-bit wide which are adressed by the program counter. Program memory can be used to store constants as well as program instructions. Three locations in Program Memory are reserved to service the two Interrupts (Timer/Counter and external) and the Reset.

Data Memory

Data memory of SAB 8048 is organized as 64 words, 8-bits wide containing the stack and 2 register banks of 8 directly addressable registers.



Timer/Counter

The internal 8-bit binary up-counter can be used to count external events and to generate accurate time delays. The increment from maximum count FF to 00 (overflow) results in the setting of an overflow flag flip-flop and in the generation of interrupt request if the interrupt is enabled.

Depending upon the type of START-Instruction used the timer/counter is clocked by the oscillator frequency: 480 or an external clock.

The timer/counter is presettable and readable with two MOV instructions.

Interrupts

The two interrupts (timer/counter an external) have the same priority. They can be enabled or disabled under program control.

Input/Output

The SAB 8048 has 27 lines which can be used for I/O functions. These lines are grouped as three 8-bit ports and three test inputs.

Port 1 and 2 are called quasi-bidirectional because each line can serve as an input, an output, or both. Port 0 is a true bidirectional port with associated input and output strobes. Input and output lines on this port cannot be mixed however.

With 4 control and strobe lines, port 0 can be used as a bidirectional bus port to interface external memory and I/O devices. The three pins T0, T1, and $\overline{\text{INT}}$ serve as inputs and are testable with conditional jump instructions.

Symbols and Abbreviations used

A	Accumulator
AC	Auxillary Carry
Adr	12-Bit Program Memory Address
An	Accumulator Bit n
BS	Bank Switch
BUS	Bus Port
CY	Carry
CLK	Clock
CNT	Event Counter
Data	8-Bit Number or Expression
DBF	Memory Bank Flip-Flop
F0, F1	Flag 0, 1
$\overline{\text{INT}}$	Interrupt
PC	Program Counter
PCn	Program Counter Bit n
Pp	Port 4-7 (for I/O-Extension with SAB 8243)
Pr	Port 1 or Port 2
PSW	Program Status Word
Rn	Register Bit n
Rr	Register 0-7
SP	Stackpointer
T	Timer
TF	Timer Flag
T0, T1	Test 0, Test 1
X	Mnemonic for External RAM
#	Immediate Data Prefix
@	Indirect Address Prefix
Page	Memory Block of 256 Byte
( )	Content
$\rightarrow$	is moved to
$\leftrightarrow$	is exchanged with
$\wedge$	logical UND
$\vee$	logical OR
$\veebar$	logical EXCLUSIV OR
–	Complement

Instruction Set

Mnemonic		Function	Description	Hex Code	Flag	Bytes	Cycles
Accumulator and Register Move Instructions							
MOV	A, Rr	(Rr) → A	Move Register Contents	F8-FF		1	1
MOV	A, @ Rr	((Rr)) → A	Move Data Memory Contents to Accumulator	F0-F1		1	1
MOV	A, # Data	Data → A	Move Immediate Data Data to Accumulator	23		2	2
MOV	A, PSW	(PSW) → A	Move PSW Contents to Accumulator	C7		1	1
MOV	PSW, A	(A) → PSW	Move Accumulator Contents to PSW	D7	CY, AC	1	1
MOV	Rr, A	(A) → Rr	Move Accumulator Contents to Register	A8-AF		1	1
MOV	@ Rr, A	(A) → (Rr)	Move Accumulator Contents to Data Memory	A0-A1		1	1
MOV	Rr, # Data	Data → Rr	Move Immediate Data to Register	B8-BF		2	2
MOV	@ Rr, # Data	Data → (Rr)	Move Immediate Data to Data Memory	B0-B1		2	2
MOVX	A, @ Rr	((Rr)) → A	Move External-Data-Memory Contents to Accumulator	80-81		1	2
MOVX	@ Rr, A	(A) → (Rr)	Move Accumulator Contents to External Data Memory	90-91		1	2
XCH	A, Rr	(Rr) ↔ (A)	Exchange Accumulator and Register Contents	28-2F		1	1
XCH	A, @ Rr	((Rr)) ↔ (A)	Exchange Accumulator and Data Memory Contents	20-21		1	1
XCHD	A, @ Rr	$((Rr))_{0-3} \leftrightarrow (A)_{0-3}$	Exchange Accumulator and Data Memory 4-Bit Data	30-31		1	1
MOVP3	A, @ A	(PV) save (A) → PC_{0-7} 011 → PC_{8-11} ((PC)) → A PC restor	Move Page 3 Data to Accumulator	E3		1	2
MOVP	A, @ A	(PC) save (A) → PC_{0-7} ((PC)) → A PC restor	Move Current Page Data to Accumulator	A3		1	2
SWAP	A	$(A)_{0-3} \leftrightarrow (A)_{4-7}$	Swap Nibble within Accumulator	47		1	1
Timer/Counter Move Instructions							
MOV	A, T	(T) → A	Move Timer/Counter Contents to Accumulator	42		1	1
MOV	T, A	(A) → T	Move Accumulator Contents to Timer/Counter	62		1	1

Mnemonic		Function	Description	Hex Code	Flag	Bytes	Cycles
Port Move Instructions							
IN	A, Pr	(Pr) → A	Input Port 1 or 2 Data to Accumulator	09-0A		1	2
OUTL	Pr, A	(A) → Pr	Output Accumulator Data to Port 1 or 2	39-3A		1	2
ANL	Pr, # Data	(Pr) ∧ Data → Pr	Logical AND Port 1-2 with Immediate Mask	99-9A		2	2
ORL	Pr, # Data	(Pr) ∨ Data → Pr	Logical OR Port 1-2 with Immediate Mask	89-8A		2	2
INS	A, BUS	(BUS) → A	Strobed Input of BUS-Data to Accumulator	08		1	2
OUTL	BUS, A	(A) → BUS	Output Accumulator Data to BUS	02		1	2
ANL	BUS, # Data	(BUS) ∧ Data → BUS	Logical AND BUS with Immediate Mask	98		2	2
ORL	BUS, # Data	(BUS) ∨ Data → BUS	Logical OR BUS with Immediate Mask	88		2	2
MOVD	A, P_P	(P_P) → A_{0-3} 0 → A_{4-7}	Move Port 4-7 Port 4 of SAB 8243 5 to Accumulator 6 7	0C 0D 0E 0F		1 1 1 1	2 2 2 2
MOVD	P_p, A	$(A)_{0-3}$ → P_p	Move Accumulator Port 4 to Port 4-7 5 of SAB 8243 6 7	3C 3D 3E 3F		1 1 1 1	2 2 2 2
ANLD	P_p, A	$(A)_{0-3}$ ∧ (P_p) → P_p	Logical AND Port 4 Port 4-7 of 5 SAB 8243 with 6 Accumulator Mask 7	9C 9D 9E 9F		1 1 1 1	2 2 2 2
ORLD	P_p, A	$(A)_{0-3}$ ∨ (P_p) → P_P	Logical OR Port 4 Port 4-7 of 5 SAB 8243 with 6 Accumulator Mask 7	8C 8D 8E 8F		1 1 1 1	2 2 2 2
Arithmetic Accumulator Instructions							
ADD	A, R_r	(A) + (R_r) → A	Add Register Contents to Accumulator	68-6F	AC, CY	1	1
ADD	A, @ R_r	(A) + ((R_r)) → A	Add Data Memory Contents to Accumulator	60 61	AC, CY	1	1
ADD	A, # Data	(A) + Data → A	Add Immediate Data to Accumulator	03	AC, CY	2	2
ADDC	A, R_r	(A) + (R_r) + (CY) → A	Add Carry and Register Contents to Accumulator	78-7F	AC, CY	1	1
ADDC	A, @ R_r	(A) +(R_r)) + (CY) → A	Add Carry and Data Memory Contents to Accumulator	70 71	AC, CY	1	1
ADDC	A, # Data	(A) + Data + (CY) → A	Add Carry and Immediate Data to Accumulator	13	AC, CY	2	2

Mnemonic		Function	Description	Hex Code	Flag	Bytes	Cycles
INC	A	(A) + 1 → A	Increment Accumulator	17		1	1
DEC	A	(A) – 1 → A	Decrement Accumulator	07		1	1
DA	A		Decimal Adjust Accumulator	57	AC, CY	1	1

Arithmetic Register Instructions

INC	R_r	$(R_r) + 1 \rightarrow R_r$	Increment Register	18–1F		1	1
DEC	R_r	$(R_r) - 1 \rightarrow R_r$	Decrement Register	C8–CF		1	1
INC	@ R_r	$((R_r)) + 1 \rightarrow (R_r)$	Increment Data Memory Location	10–11		1	1
DJNZ	R_r, Adr	$(R_r) - 1 \rightarrow R_r$ if $(R_r) \neq 0$ Adr → $PC_{0\text{-}7}$	Decrement Register and Test Register if Zero	E8–EF		2	2

Logical Accumulator and Register Instructions

ANL	A, R_r	$(A) \wedge (R_r) \rightarrow A$	Logical AND Accumulator with Register Mask	58–5F		1	1
ANL	A, @ R_r	$(A) \wedge ((R_r)) \rightarrow A$	Logical AND Accumulator with Memory Mask	50 51		1	1
ANL	A, # Data	(A) ∧ Data → A	Logical AND Accumulator with Immediate Mask	53		2	2
ORL	A, R_r	$(A) \vee (R_r) \rightarrow A$	Logical OR Accumulator with Register Mask	48–4F		1	1
ORL	A, @ R_r	$(A) \vee ((R_r)) \rightarrow A$	Logical OR Accumulator with Memory Mask	40 41		1	1
ORL	A, # Data	(A) ∨ Data → A	Logical OR Accumulator with Immediate Mask	43		2	2
XRL	A, R_r	$(A) \veebar (R_r) \rightarrow A$	Logical XOR Accumulator with Register Mask	D8–DF		1	1
XRL	A, @ R_r	$(A) \veebar ((R_r)) \rightarrow A$	Logical XOR Accumulator with Memory Mask	D0 D1		1	1
XRL	A, # Data	(A) ⊻ Data → A	Logical XOR Accumulator with Immediate Mask	D3		2	2
CLR	A	0 → A	Clear Accumulator	27		1	1
CPL	A	$\overline{(A)} \rightarrow A$	Complement Accumulator	37		1	1

Rotate Instructions

RL	A	(An) → An + 1	Rotate Accumulator Left without Carry	E7		1	1
RLC	A	(An) → An + 1 $(A_7) \rightarrow CY$ $(CY) \rightarrow A_0$	Rotate Accumulator Left through Carry	F7	CY	1	1
RR	A	(An + 1) → An	Rotate Accumulator Right without Carry	77		1	1
RRC	A	(An + 1) → An $(A_0) \rightarrow CY$ $(CY) \rightarrow A_7$	Rotate Accumulator Right through Carry	67	CY	1	1

Mnemonic		Function	Description	Hex Code	Flag	Bytes	Cycles
Flag Instructions							
CLR	C	$0 \rightarrow CY$	Clear Carry Bit	97	CY	1	1
CPL	C	$\overline{(CY)} \rightarrow CY$	Complement Carry Bit	A7	CY	1	1
CLR	F0	$0 \rightarrow F0$	Clear Flag 0	85		1	1
CPL	F0	$\overline{(F0)} \rightarrow F0$	Complement Flag 0	95		1	1
CLR	F1	$0 \rightarrow F1$	Clear Flag 1	A5		1	1
CPL	F1	$\overline{(F1)} \rightarrow F1$	Complement Flag 1	B5		1	1
Branch Instructions							
JMP	Adr	$Adr_{0-7} \rightarrow PC_{0-7}$ $Adr_{8-10} \rightarrow PC_{8-10}$ $DBF \rightarrow PC_{11}$	Direct Jump within 2K-Block Page 0 1 2 3 4 5 6 7	04 24 44 64 84 A4 C4 E4		2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2
JMPP	@ A	$((A)) \rightarrow PC_{0-7}$	Indirect Jump within Page	B3		1	2
JC	Adr	If (CY) = 1 $Adr \rightarrow PC_{0-7}$	Jump if Carry is set	F6		2	2
JNC	Adr	If (CY) = 0 $Adr \rightarrow PC_{0-7}$	Jump if Carry is not set	E6		2	2
JZ	Adr	If (A) = 0 $Adr \rightarrow PC_{0-7}$	Jump if Accumulator is Zero	C6		2	2
JNZ	Adr	If (A) $\neq$ 0 $Adr \rightarrow PC_{0-7}$	Jump if Accumulator is not Zero	96		2	2
JT0	Adr	If T0 = 1 $Adr \rightarrow PC_{0-7}$	Jump if Test 0 is High	36		2	2
JNT0	Adr	If T0 = 0 $Adr \rightarrow PC_{0-7}$	Jump if Test 0 is Low	26		2	2
JT1	Adr	If T1 = 1 $Adr \rightarrow PC_{0-7}$	Jump if Test 1 is High	56		2	2
JNT1	Adr	If T1 = 0 $Adr \rightarrow PC_{0-7}$	Jump if Test 1 is Low	46		2	2
JF0	Adr	If F0 = 1 $Adr \rightarrow PC_{0-7}$	Jump if Flag 0 is set	B6		2	2
JF1	Adr	If F1 = 1 $Adr \rightarrow PC_{0-7}$	Jump if Flag 1 is set	76		2	2
JTF	Adr	If TF = 1 $Adr \rightarrow PC_{0-7}$ $0 \rightarrow TF$	Jump if Timer Flag is set	16	TF	2	2
JNI	Adr	If $\overline{INIT}$ = 0 $Adr \rightarrow PC_{0-7}$	Jump if Interrupt input is Low	86		2	2

Mnemonic		Function	Description		Hex Code	Flag	Bytes	Cycles
JBn	Adr	If Bit n = 1 Adr → PC_{0-7}	Jump if Accumulator Bit n is set	n = 0	12		2	2
				1	32		2	2
				2	52		2	2
				3	72		2	2
				4	92		2	2
				5	B2		2	2
				6	D2		2	2
				7	F2		2	2

Subroutine Instructions

CALL	Adr	(PC_{0-11}, PSW) → (SP) (SP) + 1 → SP Adr_{0-7} → PC_{0-7} Adr_{8-10} → PC_{8-10} DBF → PC_{11}	Subroutine Call	Page 0	14		2	2
				1	34		2	2
				2	54		2	2
				3	74		2	2
				4	94		2	2
				5	B4		2	2
				6	D4		2	2
				7	F4		2	2
RET		(SP) – 1 → SP ((SP)) → PC	Return without PSW Restore		83		1	2
RETR		(SP) – 1 → SP ((SP)) → PC ((SP)) → PSW_{4-7}	Return with PSW Restore		93	AC, CY	1	2

Control Instructions

STRT	T		Start Timer	55		1	1
STRT	CNT		Start Event Counter	45		1	1
STOP	TCNT		Stop Timer/Event-Counter	65		1	1
EN	TCNTI		Enable Timer/Counter Interrupt	25		1	1
DIS	TCNTI		Disable Timer/Counter Interrupt	35		1	1
EN	I		Enable External Interrupt	05		1	1
DIS	I		Disable External Interrupt	15		1	1
SEL	RB0	0 → BS	Select Register Bank 0	C5		1	1
SEL	RB1	1 → BS	Select Register Bank 1	D5		1	1
SEL	MB0	0 → DBF	Select Memory Bank 0	E5		1	1
SEL	MB1	1 → DBF	Select Memory Bank 1	F5		1	1
ENT0	CLK		Enable Clock Output	75		1	1
NOP			The NOP Instruction	00		1	1

Absolute Maximum Ratings[1)]

Ambient Temperature Under Bias	– 40 to + 85 °C for T40/85 – 40 to + 110 °C for T40/110
Storage Temperature	– 65 to + 125 °C
Voltage On Any Pin With Respect to Ground	– 0.5 to + 7 V
Power Dissipation	1.5 W

D.C. and Operating Characteristics

$V_{CC} = V_{DD} = +5\ V \pm 10\ \%$; $V_{SS} = 0\ V$; T_A – 40 to + 85 °C for T40/85
T_A – 40 to + 110 °C for T40/110

Symbol	Parameter	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
V_{IL}	Input Low Voltage (All Except $\overline{RESET}$, XTAL1, XTAL2)	– 0.5	–	0.8	V	–
V_{IL1}	Input Low Voltage ($\overline{RESET}$, XTAL1, XTAL2)	– 0.5	–	0.6	V	–
V_{IH}	Input High Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$)	2.0	–	V_{CC}	V	–
V_{IH1}	Input High Voltage (XTAL1, XTAL2, $\overline{RESET}$)	3.8	–	V_{CC}	V	–
V_{OL}	Output Low Voltage (BUS)	–	–	0.45	V	$I_{OL} = 2.0$ mA
V_{OL1}	Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	–	–	0.45	V	$I_{OL} = 1.8$ mA
V_{OL2}	Output Low Voltage (PROG)	–	–	0.45	V	$I_{OL} = 1.0$ mA
V_{OL3}	Output Low Voltage (All Other Outputs)	–	–	0.45	V	$I_{OL} = 1.6$ mA
V_{OH}	Output High Voltage (BUS)	2.4	–	–	V	$I_{OH} = 400\ \mu A$
V_{OH1}	Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	2.4	–	–	V	$I_{OH} = 100\ \mu A$
V_{OH2}	Output High Voltage (All Other Outputs)	2.4	–	–	V	$I_{OH} = 40\ \mu A$
I_{L1}	Input Leakage Current (T1, $\overline{INT}$)	–	–	± 10	µA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{LI1}	Input Leakage Current (P10-P17, P20-P27, EA, $\overline{SS}$)	–	–	– 500	µA	$V_{SS} + 0.45 \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage Current (BUS, TO) (High Impedance State)	–	–	± 10	µA	$V_{SS} + 0.45 \le V_{IN} \le V_{CC}$
I_{DD}	V_{DD} Supply Current	–	5	15	mA	–
$I_{DD} + I_{CC}$	Total Supply Current	–	60	135	mA	–

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics

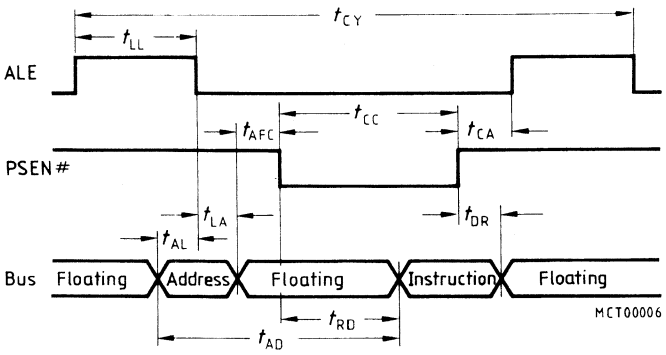
$V_{CC} = V_{DD} = +5\ V \pm 10\ \%$; $V_{SS} = 0\ V$; T_A – 40 to + 85 °C for T40/85
T_A – 40 to + 110 °C for T40/110

Symbol	Parameter	Limit Values		Unit	Test Conditions
		min.	max.		
t_{LL}	ALE Pulse Width	400	–	ns	–
t_{AL}	Address Setup to ALE	120	–	ns	–
t_{LA}	Address Hold from ALE	80	–	ns	–
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	700	–	ns	–
t_{DW}	Data Setup before $\overline{WR}$	500	–	ns	–
t_{WD}	Data Hold After $\overline{WR}$	120	–	ns	$C_L = 20$ pF
t_{CY}	Cycle Time	2.5	15.0	µs	6 MHz Crystal = 2.5 µs
t_{DR}	Data Hold	0	200	ns	–
t_{RD}	$\overline{PSEN}$, $\overline{RD}$ to Data In	–	500	ns	–
t_{AW}	Address Setup to $\overline{WR}$	230	–	ns	–
t_{AD}	Address Setup to Data In	–	950	ns	–
t_{AFC}	Address Float to $\overline{RD}$, $\overline{PSEN}$	0	–	ns	–
t_{CA}	Control Pulse to ALE	10	–	ns	–

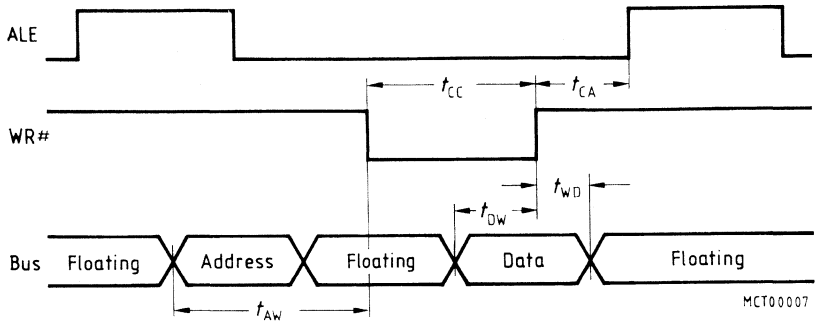
* Control outputs: $C_L = 80$ pF; BUS outputs: $C_L = 150$ pF

Waveforms

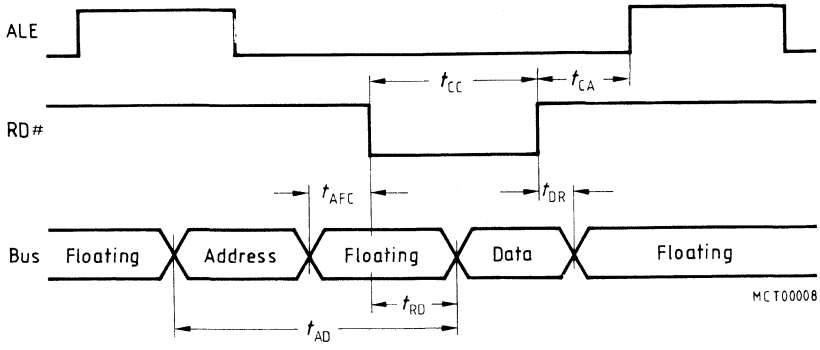
Instruction fetch from external program memory



Write to External Data Memory



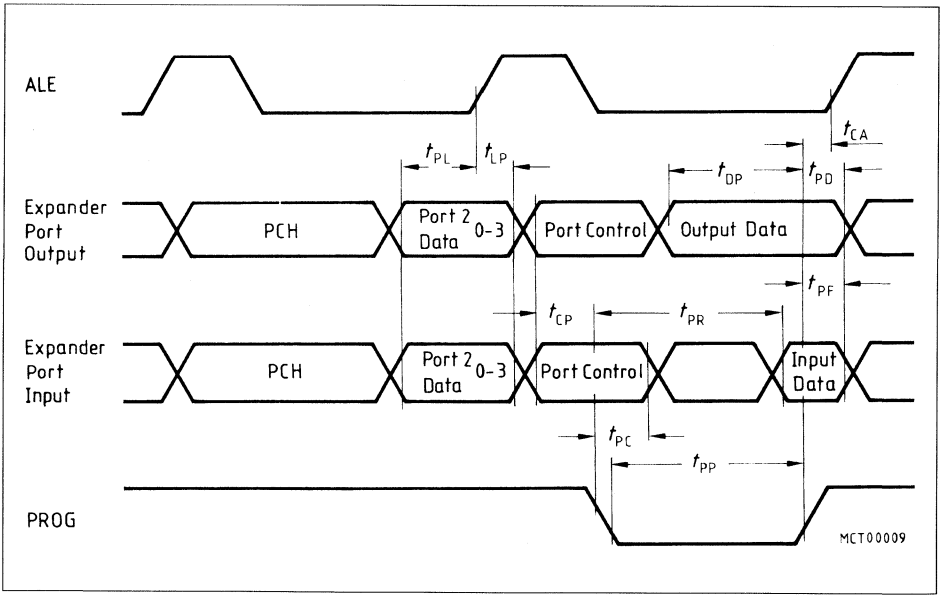
Read From External Data Memory



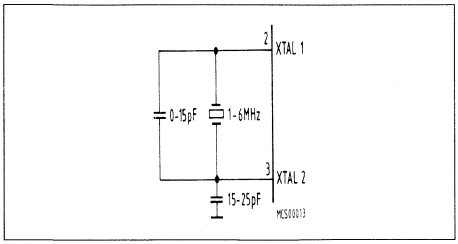
A.C. Characteristics (Port 2 Timing)

$V_{CC} = V_{DD} = +5\ V \pm 10\ \%$; $V_{SS} = 0\ V$; T_A – 40 to + 85 °C for T40/85
T_A – 40 to + 110 °C for T40/110

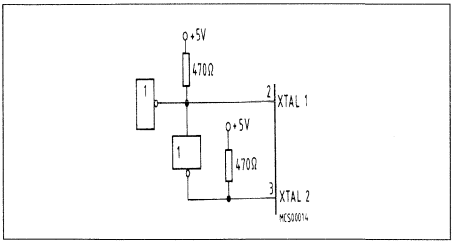
Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{CP}	Port Control Setup Before Falling Edge of PROG	110	–	ns
t_{PC}	Port Control Hold After Falling Edge of PROG	100	–	ns
t_{PR}	PROG to Time P2 Input Must Be Valid	–	810	ns
t_{PF}	Input Data Hold Time	0	150	ns
t_{DP}	Output Data Setup Time	250	–	ns
t_{PD}	Output Data Hold Time	65	–	ns
t_{PP}	PROG Pulse Width	1200	–	ns
t_{PL}	Port 2 I/O Data Setup	350	–	ns
t_{LP}	Port 2 I/O Data Hold	150	–	ns



Connecting the Oscillator Inputs



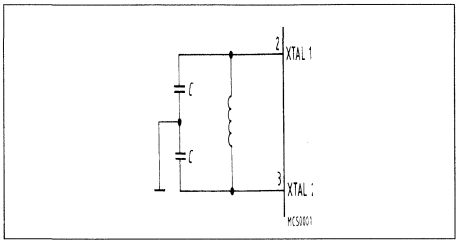
Crystal series resistance should be
< 75 Ω at 6 MHz and < 180 Ω at 3.6 MHz.



Both XTAL1 and XTAL2 should be driven.

Resistors to V_{CC} are needed to ensure V_{IH} = 3.8 V if TTL circuitry is used.

XTAL1 and XTAL2 must be high 35-65 % of the period.



$$f = \frac{1}{2\pi\sqrt{LC'}} \qquad C' = \frac{C + 3\,C_{PP}}{2}$$

$C_{PP} \approx$ 5-10 pF pin-to-pin capacitance

Ordering Information

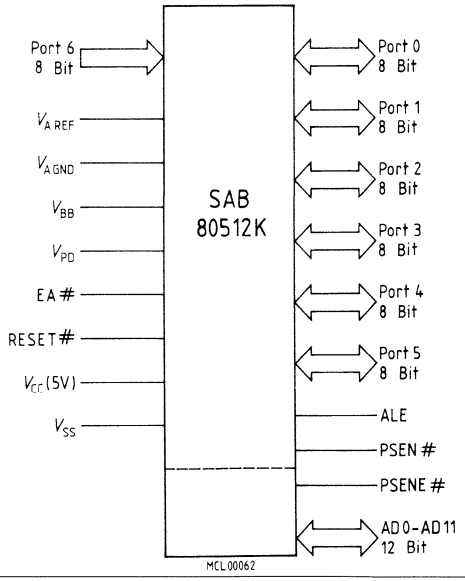
Type	Ordering code	Function
		8 Bit Single-Chip-Microcomputer
SAB 8048-P-T40/85	Q67120-C133	with maskprogrammable ROM (Plastic)
SAB 8048-P-T40/110	Q67120-C162	with maskprogrammable ROM (Plastic)
SAB 8035L-P-T40/85	Q67120-C140	with external ROM (Plastic)

8-Bit Single-Chip Microcontroller — SAB 80512K
ROM-less Version

Obsolescent Type

- Additional bus interface for external memory
- 128 × 8 RAM
- Full upward compatibility to SAB 8051A/8031A
- Seven 8-bit ports
- Two 16-bit timer/event counters
- High-performance full-duplex serial channel with dedicated baud rate generator
- Six interrupt sources (2 external, 4 internal), two priority levels progammable
- 8-bit A/D converter with eight multiplexed inputs, reference voltages externally adjustable
- Boolean processor
- 1 µs instruction cycle time (at 12 MHz oscillator frequency)
- 4 µs multiply and divide (at 12 MHz oscillator frequency)
- External program and data memory expandable to 64 Kbyte each
- Pin grid array package, 88 pins (C-PGA-88)

Logic Symbol



Ordering Information

Type	Ordering code	Function
SAB 80512K-A	Q67120-C333	8-bit single-chip microcontroller ROM-less version

The SAB 80512K is a ROM-less version of the 8-bit microcontroller SAB 80512. It contains an additional bus interface to connect an external program memory in place of the SAB 80512's on-chip ROM.Thereby,the SAB 80512K maintains the full I/O capability of the single-chip SAB 80512 while it permits connection of an external memory. All other features of the SAB 80512K are identical with the SAB 80512. The SAB 80512K is fabricated in + 5 V advanced N-channel, silicon gate Siemens MYMOS technology, and supplied as pin grid array with 88 pins (C-PGA-88).

SIEMENS

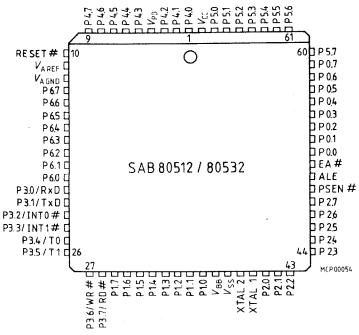
8-Bit Single-Chip Microcontroller — SAB 80512/80532

Obsolescent Type

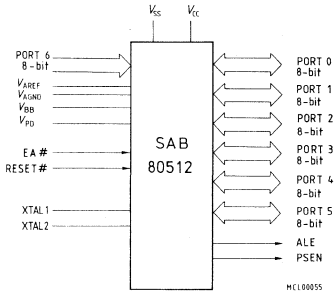
SAB 80512-N Microcontroller with factory-maskprogrammable ROM
SAB 80532-N Microcontroller for external ROM

- 4 K × 8 ROM (SAB 80512 only)
- 128 × 8 RAM
- Full backward compatibility to SAB 8051A/8031A
- Seven 8-bit ports
- Two 16-bit timers/event counters
- High performance full duplex serial channel with own baud rate generator
- 8-bit A/D converter with eight multiplexed inputs, reference voltages externally adjustable
- Six interrupt sources (2 external, 4 internal), two priority levels programmable
- Boolean processor
- 1 µs instruction cycle time (at 12 MHz osc. frequency)
- 4 µs multiply and divide (at 12 MHz osc. frequency)
- External program and data memory expandable up to 64 Kbyte each
- PL-CC-68 package

Pin Configurations



Logic Symbol



The SAB 80512/80532 is a new member of the Siemens SAB 8051 family of 8-bit microcontrollers. Maintaining all features of the SAB 8051A/8031A, it is fully backward compatible to the SAB 8051A/8031A. Furthermore the SAB 80512/80532 incorporates several enhancements that significantly increase design flexibility and cost effectiveness. Compared to the SAB 8051A/8031A the SAB 80512/ 80532 additionally contains an 8-bit A/D converter with 8 multiplexed inputs (these inputs can also be used as digital inputs), an own baud rate generator for the serial interface and two more I/O ports.The SAB 80532 is identical with the SAB 80512, except that it lacks the on-chip ROM.
The SAB 80512/80532 is fabricated in + 5 V advanced N-channel, silicon gate MYMOS technology of Siemens and supplied in a PL-CC-68 package. For the industrial temperature range – 40 to + 85°C, the SAB 80512/80532-T40/85 is available.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	I/O	Port 4 is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 4 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors.
V_{PD}	4	–	Power down supply voltage. If V_{PD} is held within its specifications while V_{CC} drops below the specification, V_{PD} will providestandby power to 40 byte of internal RAM (addr. 58H to 7FH).During normal operation of the SAB 80512, the RAM's current is supplied by V_{CC}, when V_{PD} is low.
$\overline{\text{RESET}}$	10	I	A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80512. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	11	–	Reference voltage for the A/D converter
V_{AGND}	12	–	Reference ground for the A/D converter
P6.7-P6.0	13-20	I	Port 6, 8-bit unidirectional input port. Port pins can be used for digital input if voltage levels meet the specified input high/low voltages and for the eight multiplexed analog inputs of the A/D converter, simultaneously.
P3.0-P3.7	21-28	I/O	Port 3 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs port 3 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. It also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – RxD (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – TxD (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{\text{INT0}}$ (P3.2): interrupt 0 input/timer 0 gate control input – $\overline{\text{INT1}}$ (P3.3): interrupt 1 input/timer 1 gate control – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{\text{WR}}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{\text{RD}}$ (P3.7): the read control signal enables the external data memory to port 0

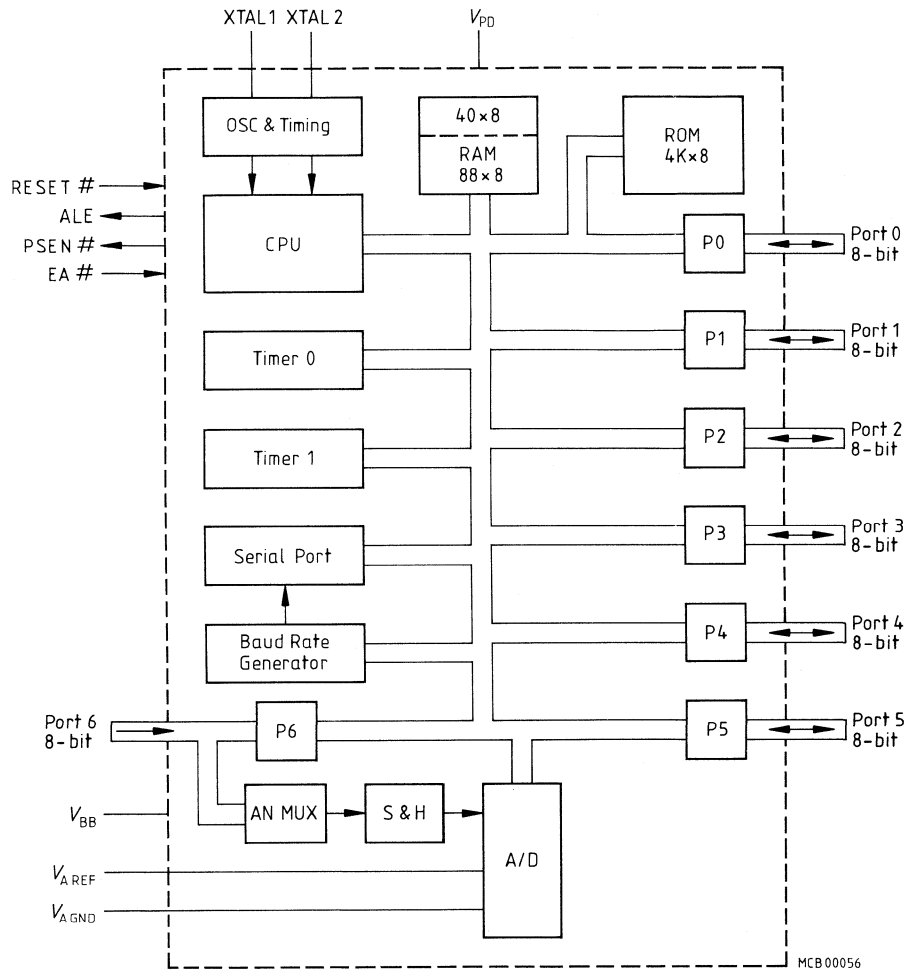
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P1.7-P1.0	29-36	I/O	Port 1 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs port 1 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. The port is also used for the low order address byte during program verification.
V_{BB}	37	–	Substrate pin. Must be connected to V_{SS} with a capacitor (100 nF to 1000 nF) for proper operation of the A/D converter.
XTAL2 XTAL1	39 40	– –	XTAL2 Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is pulled low. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times specified in the AC characteristics must be observed: XTAL1 Input to the inverting oscillator amplifier. Required when a crystal or ceramic resonator is used.
P2.0-P2.7	41-48	I/O	Port 2 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs port 2 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application it uses strong internal pullup resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	49	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periodes except during external data memory accesses. Remains high during internal program execution.
ALE	50	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periodes except during an external data memory access.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{EA}$	51	I	When held at a TTL high level, the SAB 80512 executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the SAB 80512 fetches all instructions from external program memory. For the SAB 80532 this pin must be tied low.
P0.0-P0.7	52-59	I/O	Port 0 is an 8-bit open drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1s. Port 0 also outputs the code bytes during program verification. External pullup resistors are required during program verification.
P5.7-P5.0	60-67	I/O	Port 5 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 5 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs port 5 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors.
V_{CC}	68	–	Supply voltage during normal operation and program verification.
V_{SS}	38	–	Ground (0 V)

Block Diagram



Functional Description

The SAB 80512/80532 is based on the architecture of the SAB 8051 microcontroller family. The SAB 80512 includes all features of the SAB 8051 and additionally offers peripheral extensions in three items:

- bit A/D converter with adjustable reference voltage
- two more ports
- dedicated baud rate generator

Different to the SAB 8051 is the inverted reset-input and the RAM power-down supply by a special pin (V_{PD}), which supplies 40 byte with a typical current of 2 mA. Beside the backward compatibility to the SAB 8051 (all SAB 8051 software runs on the SAB 80512 without any changes) the SAB 80512 is also upwardly compatible to the SAB 80515. The SAB 80512 is packed into the PL-CC-68 package and has got the same pinning as the SAB 80515.

A/D Converter

The 8-bit A/D converter of the SAB 80512 has 8 multiplexed analog inputs and uses the successive approximation method. The sampling of an analog signal takes 5 machine cycles, the total conversion time is 15 machine cycles (15 µs at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous, at the end of a conversion an interrupt can be generated. The SAB 80512 provides variable external reference voltages V_{AGND} and V_{AREF} adjustable in a wide range. A compressed reference voltage range allows to increase the resolution of the converted analog input. The lower reference voltage (V_{AGND}) can be varied within V_{SS} – 0.2 V and 4 V, the higher (V_{AREF}) within 1 V and V_{CC} + 5%. For proper operation of the A/D converter a minimum of 1 V difference is required between the external voltages:

$(V_{SS} - 0.2\ V) \leq V_{AGND} \leq (V_{AREF} - 1\ V)$

$(V_{AGND} + 1\ V) \leq V_{AREF} \leq (V_{CC} + 5\%)$

Special Function Register

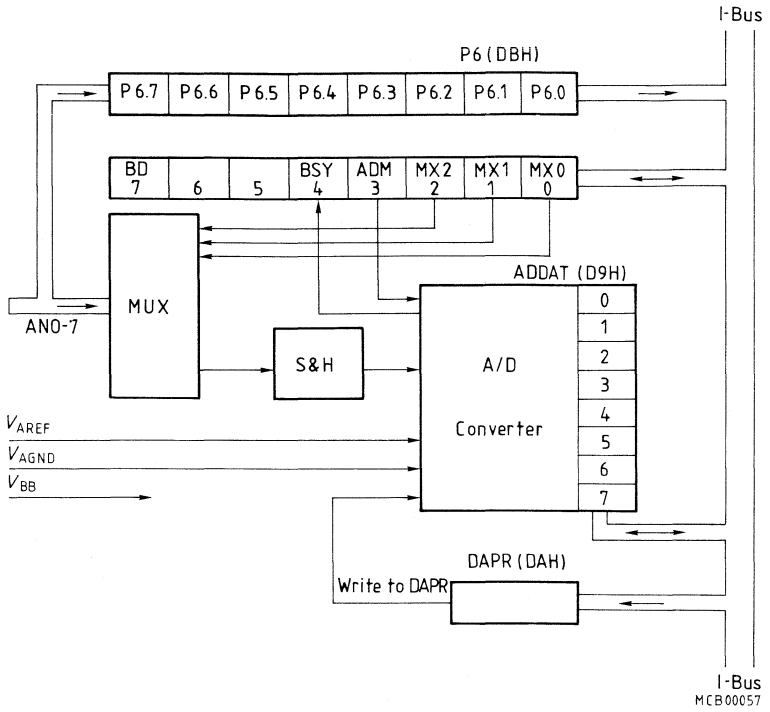
All registers, except the program counter and the four 8-register banks, reside in the special function register area. The 28 special function registers (SFRs) include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripheral functions. There are also 128 directly addressable bits within the SFR area

I/O Ports

The SAB 80512 has six 8-bit I/O ports and one 8-bit input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pullups. That means, when configured as inputs, ports 1 to 5 will pull high and will source current when externally pulled low. Port 0 will float when configured as input. Port 6 is an input port only and can be used as digital input port, if the values meet the specified high/low voltages and as analog input for the A/D-converter.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.

Block Diagram of A/D Converter



Special Function Registers

Address	Symbol	Name	bit-addressable
80H	P0	Port 0 Register	yes
81H	SP	Stack Pointer	–
82H	DPL	Data Pointer, low-byte	–
83H	DPH	Data Pointer, high-byte	–
87H	PCON	Power Control Register	–
88H	TCON	Timer Control Register	yes
89H	TMOD	Timer Mode Register	–
8AH	TL0	Timer 0, low-byte	–
8BH	TL1	Timer 1, low-byte	–
8CH	TH0	Timer 0, high-byte	–
8DH	TH1	Timer 1, high-byte	–
90H	P1	Port 1 Register	yes
98H	SCON	Serial Port Control Register	yes
99H	SBUF	Serial Port Buffer Register	–
0A0H	P2	Port 2 Register	yes
0A8H	IE	Interrupt Enable Register	yes
0B0H	P3	Port 3 Register	yes
0B8H	IP	Interrupt Priority Register	yes
0C0H	IRCON	Interrupt Request Control	yes
0D0H	PSW	Program Status Word Register	yes
0D8H	ADCON	A/D Converter Control Register	yes
0D9H	ADDAT	A/D Converter Data Register	–
0DAH	DAPR	D/A Converter Start Register	–
0DBH	P6	Port 6 Register	–
0E0H	ACC	Accumulator Register	yes
0E8H	P4	Port 4 Register	yes
0F0H	B	B-Register	yes
0F8H	P5	Port 5 Register	yes

Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
ANL	direct,#data	AND immediate data to direct byte	3	1
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct, A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct, A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct*)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct, A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct byte and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn	–	Working register R0-R7
direct	–	128 internal RAM locations, any I/O port, control or status register
@Ri	–	Indirect internal or external RAM location addressed by register R0 or R1
#data	–	8-bit constant included in instruction
#data 16	–	16-bit constant included as bytes 2 and 3 of instruction
bit	–	128 software flags, any I/O pin, control or status bit
A	–	Accumulator

Notes on program addressing modes:

addr 16	–	Destination address for LCALL and LJMP may be anywhere within the 64-Kbyte program memory address space.
addr 11	–	Destination address for ACALL and AJMP will be within the same 2-Kbyte page of program memory as the first byte of the following instruction.
rel	–	SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/– 128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	addr. 11
02	3	LJMP	addr. 16
03	1	RR	A
04	1	INC	A
05	2	INC	direct
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit,rel*
11	2	ACALL	addr. 11
12	3	LCALL	addr. 16
13	1	RRC	A
14	1	DEC	A
15	2	DEC	direct
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit,rel*
21	2	AJMP	addr. 11
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,direct
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit,rel*
31	2	ACALL	addr. 11
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,#data
35	2	ADDC	A,direct
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R6
3F	1	ADDC	A,R7
40	2	JC	*rel*
41	2	AJMP	addr. 11
42	2	ORL	direct,A
43	3	ORL	direct,#data
44	2	ORL	A,#data
45	2	ORL	A,direct
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*rel*
51	2	ACALL	addr. 11
52	2	ANL	direct,A
53	3	ANL	direct,#data
54	2	ANL	A,#data
55	2	ANL	A,direct
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*rel*
61	2	AJMP	addr. 11
62	2	XRL	direct,A
63	3	XRL	direct,#data
64	2	XRL	A,#data
65	2	XRL	A,direct
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*rel*
71	2	ACALL	*addr. 11*
72	2	ORL	C,*bit*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*direct*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*rel*
81	2	AJMP	*addr. 11*
82	2	ANL	C,*bit*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*direct, direct*
86	2	MOV	*direct*,@R0
87	2	MOV	*direct*,@R1
88	2	MOV	*direct*,R0
89	2	MOV	*direct*,R1
8A	2	MOV	*direct*,R2
8B	2	MOV	*direct*,R3
8C	2	MOV	*direct*,R4
8D	2	MOV	*direct*,R5
8E	2	MOV	*direct*,R6
8F	2	MOV	*direct*,R7
90	3	MOV	DPTR,#*data 16*
91	2	ACALL	*addr. 11*
92	2	MOV	*bit*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*direct*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	A,*bit #*
A1	2	AJMP	*addr. 11*
A2	2	MOV	C,*bit*
A3	1	INC	DPTR
A4	1	MUL	AB
A5	2	reserved	
A6	2	MOV	@R0,*direct*
A7	2	MOV	@R1,*direct*
A8	2	MOV	R0,*direct*
A9	2	MOV	R1,*direct*
AA	2	MOV	R2,*direct*
AB	2	MOV	R3,*direct*
AC	2	MOV	R4,*direct*
AD	2	MOV	R5,*direct*
AE	2	MOV	R6,*direct*
AF	2	MOV	R7,*direct*
B0	2	ANL	C,/*bit*
B1	2	ACALL	*addr. 11*
B2	2	CPL	*bit*
B3	1	CPL	C
B4	3	CJNE	A,#*data,rel*
B5	3	CJNE	A,*direct,rel*
B6	3	CJNE	@R0,#*data,rel*
B7	3	CJNE	@R1,#*data,rel*
B8	3	CJNE	R0,#*data,rel*
B9	3	CJNE	R1,#*data,rel*
BA	3	CJNE	R2,#*data,rel*
BB	3	CJNE	R3,#*data,rel*
BC	3	CJNE	R4,#*data,rel*
BD	3	CJNE	R5,#*data,rel*
BE	3	CJNE	R6,#*data,rel*
BF	3	CJNE	R7,#*data,rel*
C0	2	PUSH	*direct*
C1	2	AJMP	*addr. 11*
C2	2	CLR	*bit*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*direct*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*direct*
D1	2	ACALL	*addr. 11*
D2	2	SETB	*bit*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*direct,rel*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*rel*
D9	2	DJNZ	R1,*rel*
DA	2	DJNZ	R2,*rel*
DB	2	DJNZ	R3,*rel*
DC	2	DJNZ	R4,*rel*
DD	2	DJNZ	R5,*rel*
DE	2	DJNZ	R6,*rel*
DF	2	DJNZ	R7,*rel*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*addr. 11*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*direct**)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*addr. 11*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*direct,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Temperature under bias	0 to + 70°C for the SAB 80512/80532
	− 40 to + 85°C for the SAB 80512/80532-T40/85
storage temperature	− 65 to +150°C
Voltage on any pin with respect to ground (V_{SS})	− 0.5 to + 7 V
Power dissipation	2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5 V ±10%; V_{SS} = 0 V;
T_A = 0 to 70°C; for SAB 80512/80532
T_A = − 40 to + 85°C for SAB 80512/80532-T40/85

Symbol	Parameter	Limit Values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	− 0.5	0.8	V	–
V_{IH}	Input high voltage (except $\overline{\text{RESET}}$ and XTAL2)	2.0	V_{CC} + 0,5	V	–
V_{IH1}	Input high voltage to XTAL2	2.5	V_{CC} + 0.5	V	XTAL1 to V_{SS}
V_{IH2}	Input high voltage to $\overline{\text{RESET}}$	3.0	–	V	–
V_{PD}	Power-down voltage	3	5.5	V	V_{CC} = 0 V
V_{OL}	Output low voltage, ports 1, 2, 3, 4, 5	–	0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output low voltage, port 0, ALE, $\overline{\text{PSEN}}$	–	0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output high voltage, ports 1, 2, 3, 4, 5	2.4	–	V	I_{IOH} = − 80 µA
V_{OH1}	Output high voltage, port 0, ALE, $\overline{\text{PSEN}}$	2.4	–	V	I_{OH} = − 400 µA
I_{IL}	Logic 0 input current, ports 1, 2, 3, 4, 5	–	− 500	µA	V_{IL} = 0.45 V
I_{IL2}	Logic 0 input current, XTAL2	–	− 2.5	mA	XTAL1 = V_{SS} V_{IL} = 0.45 V
I_{IL3}	Input low current to $\overline{\text{RESET}}$ for reset	–	− 500	µA	V_{IL} = 0.45 V
I_{LI}	Input leakage current to port 0, $\overline{\text{EA}}$	–	± 10	µA	0 V < V_{IN} < V_{CC}
I_{CC}	Power supply current SAB 80512/80532 SAB 80512/80532-T40/85	–	175	mA	all outputs disconnected
I_{PD}	Power-down current	–	3	mA	V_{CC} = 0 V
C_{IO}	Capacitance of I/O buffer	–	10	pF	f_c = 1 MHz

A/D Converter Characteristics

V_{CC} = 5 V ±10%; V_{SS} = 0 V;
(V_{SS} – 0.2 V) ≤ V_{AGND} ≤ (V_{AREF} – 1 V); (V_{AGND} +1 V) ≤ V_{AREF} ≤ (V_{CC} +5%);
T_A = 0 to 70°C for SAB 80512/80532
T_A = – 40 to + 85°C for SAB 80512/80532-T40/85

Symbol	Parameter	Limit Values			Unit	Test condition
		min.	typ.	max.		
V_{AINPUT}	Analog input voltage	V_{AGND} – 0.2	–	V_{AREF} + 0.2	V	–
C_I	Analog input capacitance	–	25	70	pF	1)
t_L	Load time	–	–	2 t_{CY}	µs	
t_S	Sample time (incl. load time)	–	–	5 t_{CY}	µs	
t_C	Conversion time (incl. sample time)	–	–	15 t_{CY}	µs	
DNLE	Differential non-linearity	–	± 1/4	± 1/2	LSB	$V_{AREF} = V_{CC}$ $V_{AGND} = V_{SS}$
INLE	Integral non-linearity	–	± 1/4	± 1/2		
	Offset error	–	± 1/4	± 1/2		
	Gain error	–	± 1/4	± 1/2		
TUE	Total unadjusted error	–	± 1	± 1/2		1) 2)
I_{REF}	V_{AREF} supply current	–	–	5	mA	2)

1) The output impedance of the analog source must be low enough to assure full loading of the sample capacitance (C_I) during load time (t_L). After charging of the internal capacitance (C_I) in the load time (t_L) the analog input must be held constant for the rest of the sample time (t_S).

2) The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

AC Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V
T_A = 0 to 70°C for SAB 80512/80532
T_A = – 40 to + 85°C for SAB 80512/80532-T40/85
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock 1/ t_{CLCL} = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{CY}	Cycle time	1000	–	12 t_{CLCL}	–	ns
t_{LHLL}	ALE pulse width	127	–	2 t_{CLCL} – 40	–	ns
t_{AVLL}	Address setup to ALE	53	–	t_{CLCL} – 30	–	ns
t_{LLAX1}	Address hold after ALE	48	–	t_{CLCL} – 35	–	ns
t_{LLIV}	Address to valid instr in	–	233	–	4 t_{CLCL} – 100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	58	–	t_{CLCL} – 25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	3 t_{CLCL} – 35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instr in	–	150	–	3 t_{CLCL} – 100	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float after $\overline{PSEN}$	–	63	–	t_{CLCL} – 20	ns
t_{PXAV}*)	Address valid after $\overline{PSEN}$	75	–	t_{CLCL} – 8	–	ns
t_{AVIV}	Address to valid instr in	–	302	–	5 t_{CLCL} – 115	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

*) Interfacing the SAB 80512 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

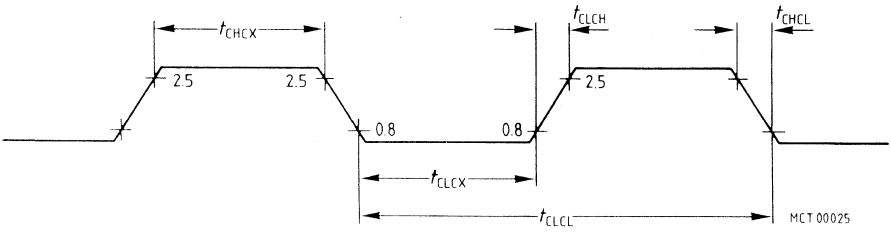
External Data Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{TCLCL}$ = 1.2 MHz to 12		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	400	–	6 t_{CLCL} – 100	–	ns
t_{WHLH}	$\overline{WR}$ pulse width	400	–	6 t_{CLCL} – 100	–	ns
t_{LLAX2}	Address hold after ALE	132	–	2 t_{CLCL} – 35	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	250	–	5 t_{CLCL} – 165	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	2 t_{CLCL} – 70	ns
t_{LLDV}	ALE to valid data in	–	517	–	8 t_{CLCL} – 150	ns
t_{AVDV}	Address to valid data in	–	585	–	9 t_{CLCL} – 165	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	4 t_{CLCL} – 130	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	t_{CLCL} – 40	t_{CLCL} + 40	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	33	–	t_{CLCL} – 50	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	7 t_{CLCL} – 150	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	t_{CLCL} – 50	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

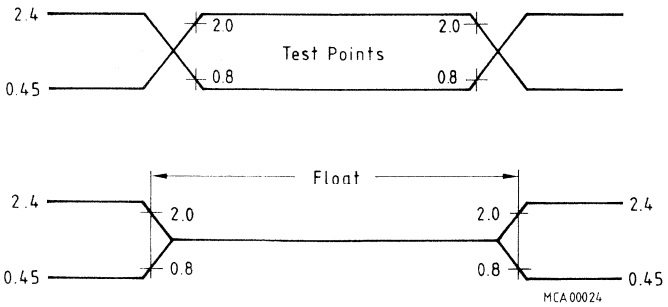
External Clock Drive XTAL2

Symbol	Parameter	Limit Values		Unit
		Variable clock Freq. = 1.2 MHz to 12 MHz		
t_{CLCL}	Oscillator period	83.3	833.3	ns
t_{CHCX}	High time	20	$t_{CLCL} - t_{CLCX}$	ns
t_{CLCK}	Low time	20	$t_{CLCL} - t_{CHCX}$	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

External Clock Cycle



AC Testing Input, Output, Float Waveforms



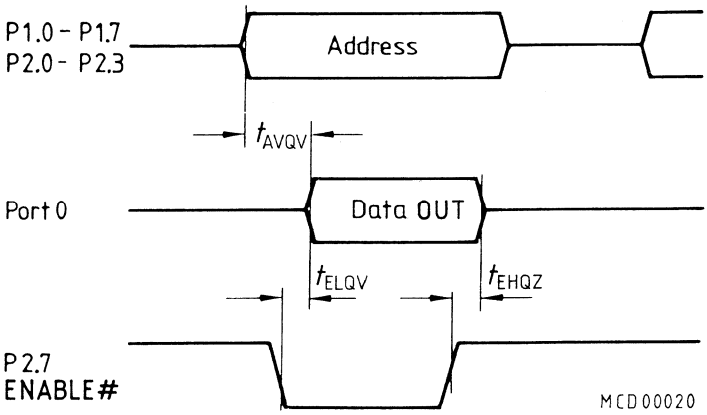
AC testing inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point where a P0 pin sinks 3.2 mA or sources 400 µA at voltage test levels.

ROM Verification Characteristics

$T_A = 25°C \pm 5°C$; $V_{CC} = 5\ V \pm 10\%$; $V_{SS} = 0\ V$

Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	ENABLE to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after ENABLE	0	48 t_{CLCL}	ns
$1 / t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification

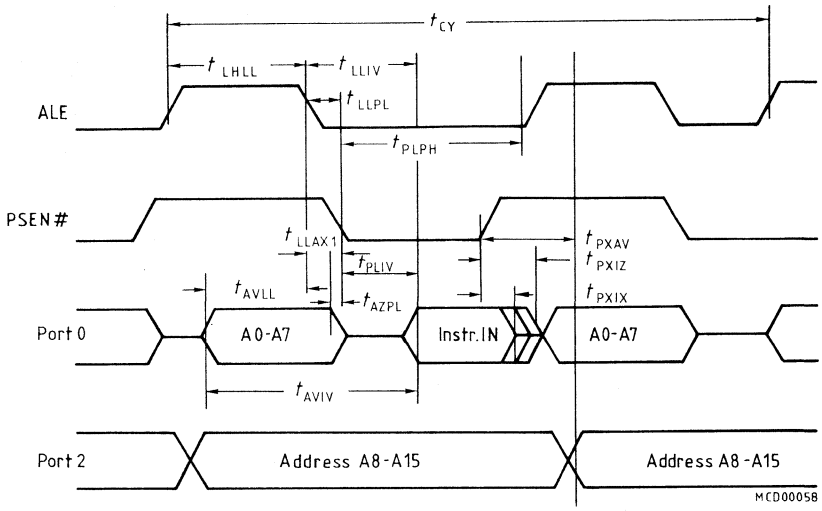


Data : P1.0-P1.7 = A0-A7
P2.0-P2.3 = A8-A11
Port 0 = D0-D7

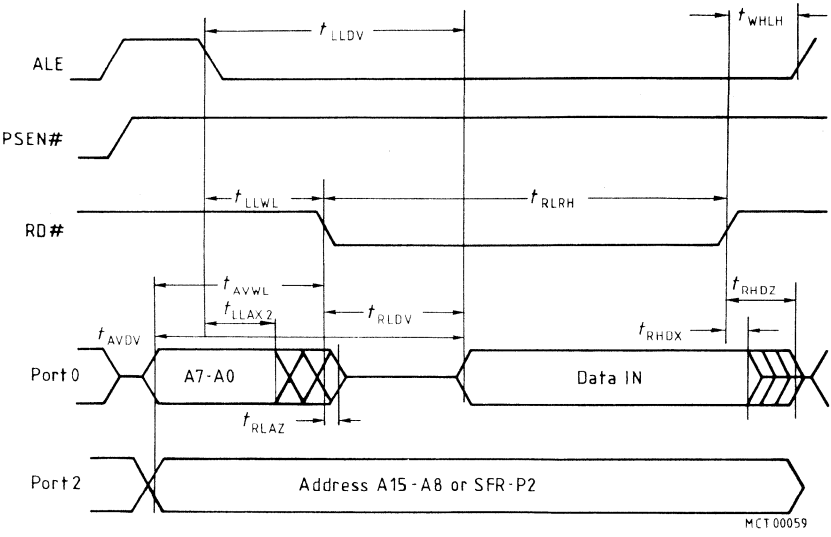
Inputs: P2.4-P2.6, $\overline{PSEN} = V_{SS}$
ALE, $\overline{EA} = V_{IH}$
$\overline{RESET} = V_{IL}$

Waveforms

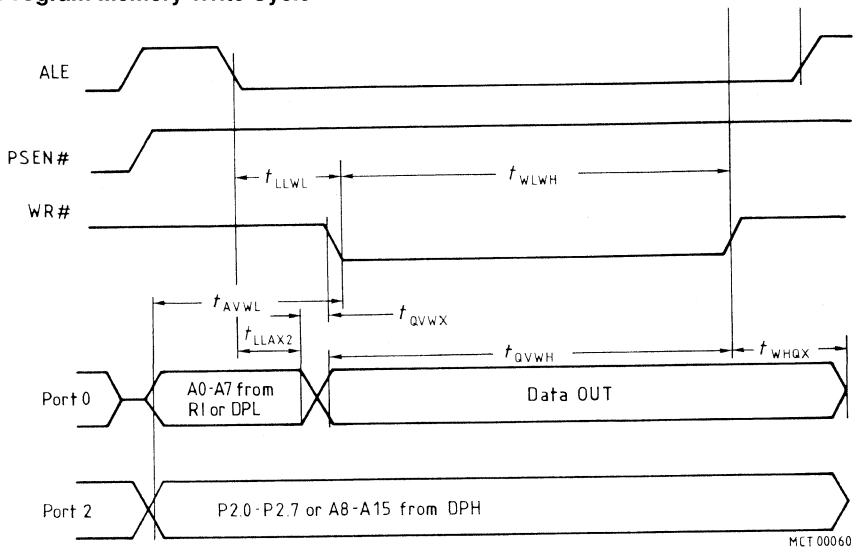
Program Memory Read Cycle



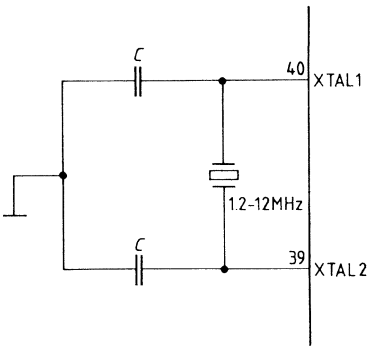
Data Memory Read Cycle



Program Memory Write Cycle

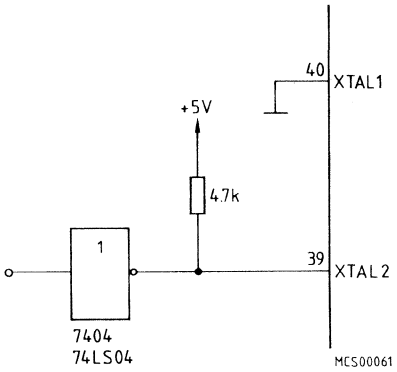


Recommended Oscillator Circuits



$C = 30\,pF \pm 10\,pF$

Crystal Oscillator Mode



Driving from External Source

Ordering Information

Type	Ordering code	Function
SAB 80512-N	Q67120-C336	8-bit single-chip microcontroller with ROM
SAB 80532-N	Q67120-C337	8-bit single-chip microcontroller for external ROM
SAB 80512-T40/85-N	Q67120-C353	like SAB 80512 but for – 40 to + 85°C
SAB 80532-T40/85-N	Q67120-C354	like SAB 80532 but for – 40 to + 85°C

8-Bit Single Chip Microcontroller

SAB 80513/80513-16
SAB 8352-5/8352-5-16

Preliminary Data

SAB 80513/80513-16 Microcontroller with 16 Kbyte ROM (12 MHz/16 MHz)
SAB 8352-5/8352-5-16 Microcontroller with 32 Kbyte ROM (12 MHz/16 MHz)

- 16 K x 8 ROM (SAB 80513)
- 32 K x 8 ROM (SAB 8352-5)
- 256 X 8 RAM
- Four 8-bit I/O ports
- Three 16-bit timer/event counters
- High performance full-duplex serial channel with flexible transmit/receive baud rate capability
- Six interrupt vectors, two priority levels are programmable
- Boolean processor
- Most instructions execute in 1 µs (750 ns)
- 4 µs (3 µs) multiply and divide
- External memory expandable up to 128 Kbytes
- Fully backward compatible to SAB 8051A and SAB 8052A/B
- Package: P-DIP-40 and PL-CC-44
- Two temperature ranges available
  - 0 to 70 °C
  - T3: – 40 to 85 °C

The SAB 80513 and SAB 8352-5 are new members of the Siemens SAB 8051 family of 8-bit microcontrollers. They are fabricated in N-channel, silicon-gate Siemens MYMOS technology.

The SAB 80513 and the SAB 8352-5 are stand-alone, high-performance, single chip microcontrollers based on the SAB 8051 architecture. Both devices maintain all features of the SAB 8051A and SAB 8052A/B (including Timer 2 of the SAB 8052A/B) and thus are fully compatible to both the SAB 8051A and SAB 8052A/B.

In addition, the SAB 80513 contains 16 Kbytes of on-chip ROM; the SAB 8352-5 contains 32 Kbyte of on-chip ROM. This feature makes very cost-effective microcontrollers for applications requiring more ROM space.

Furthermore, both parts contain 256-byte on-chip RAM, four 8-bit ports, a powerful interrupt structure with six vectors and two programmable priority levels, a serial interface as well as on-chip oscillator and clock circuitry.

Both parts are available in a 12 MHz version and in a 16 MHz version which offers an additional performance increase of 33 %.

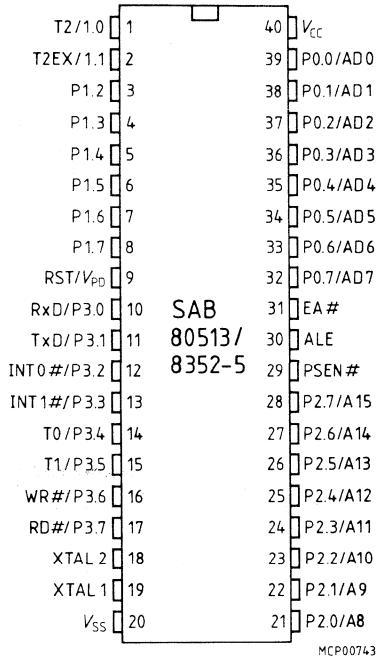
The SAB 80513 and the SAB 8352-5 are supplied in a 40-pin plastic dual-in-line (P-DIP-40) package or a 44-pin plastic leaded chip carrier (PL-CC-44) package.

The parts are available for standard temperature range (0 to 70 °C) and extended temperature range (T3: – 40 to 85 °C).

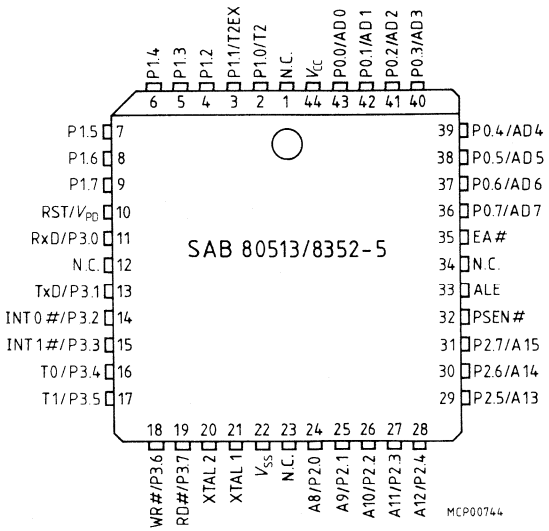
Ordering Information

Type	Ordering code	Package	Function (8-bit single-chip microcontroller)
SAB 80513-P	Q67120-C383	P-DIP-40	with 16-KByte mask-programmable ROM
SAB 80513-N	Q67120-C384	PL-CC-44	with 16-KByte mask-programmable ROM
SAB 80513-16-P	Q67120-C441	P-DIP-40	with 16-KByte mask-programmable ROM, 16 MHz
SAB 80513-16-N	Q67120-C443	PL-CC-44	with 16-KByte mask-programmable ROM, 16 MHz
SAB 80513-16-P-T3	Q67120-C506	P-DIP-40	with 16-KByte mask-programmable ROM, 16 MHz, ext. Temp.
SAB 8352-5-P	Q67120-C526	P-DIP-40	with 32-KByte mask-programmable ROM
SAB 8352-5-N	Q67120-C524	PL-CC-44	with 32-KByte mask-programmable ROM
SAB 8352-5-16-P	Q67120-C529	P-DIP-40	with 32-KByte mask-programmable ROM, 16 MHz
SAB 8352-5-16-N	Q67120-C533	PL-CC-44	with 32-KByte mask-programmable ROM, 16 MHz
SAB 8352-5-16-P-T3	Q67120-C531	P-DIP-40	with 32-KByte mask-programmable ROM, 16 MHz, ext. Temp.

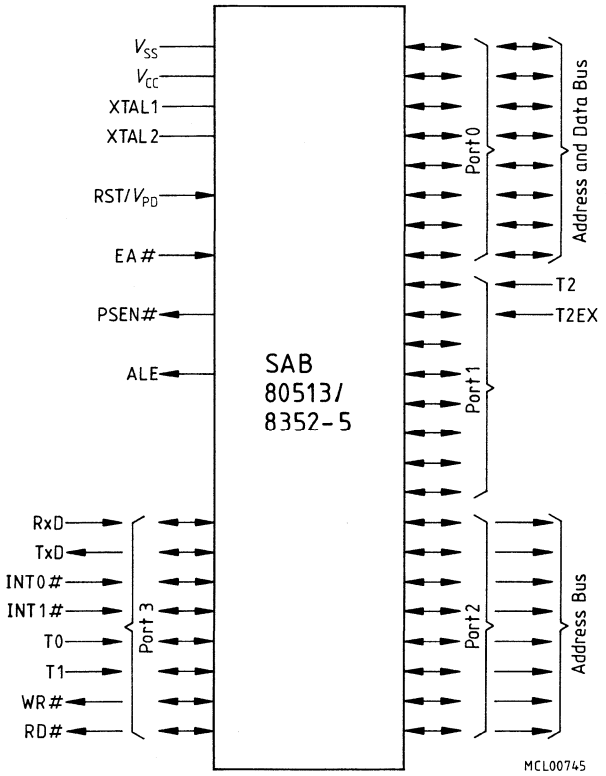
Pin Configuration
P-DIP-40



PL-CC-44



Logic Symbol



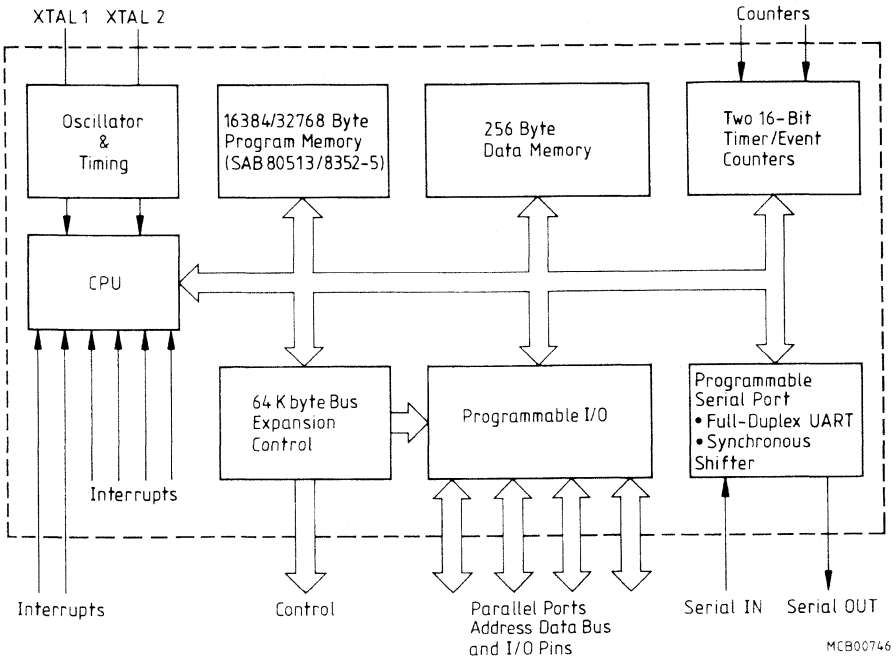
Pin Definitions and Functions

Symbol	Pin Number		Input (I) Output(O)	Function
	P-DIP-40	PL-CC-44		
P1.0-P1.7	1–8	2–9	I/O	**Port 1** is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads. Pins P1.0 and P1.1 also correspond to the special functions T2, external input to timer 2, and T2EX, timer 2 trigger input. The output latch on these two special function pins must be programmed to a one (1) for that function to operate.
RST/V_{PD}	9	10	I	**RESET** input. A high level on this pin resets the SAB 80513/8352-5. A small internal pulldown resistor permits power-on reset using only a capacitor connected to V_{CC}. If V_{PD} is held within its spec while V_{CC} drops below spec, V_{PD} will provide standby power to the RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
P3.0-P3.7	10–17	11, 13–19	I/O	**Port 3** is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and RD# and WR# pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of port 3, as follows: – RxD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TxD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – INT0# (P3.2). Interrupt 0 input or gate control input for counter 0. – INT1# (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – WR# (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – RD# (P3.7). The read control signal enables external data memory to port 0.

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		Input (I) Output(O)	Function
	P-DIP-40	PL-CC-44		
XTAL1 XTAL2	19 18	21 20	–	**XTAL1** input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to V_{SS} when external source is used on XTAL2. **XTAL2** output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0-P2.7	21-28	24-31	I/O	**Port 2** is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/ source four LS TTL loads.
PSEN#	29	32	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	33	O	The **Address Latch Enable** output is used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
EA#	31	35	I	**External Access** enable. When this pin is held on high level, the SAB 80513 executes instructions from the internal ROM when the PC is less than 4000H. When this pin is held on high level, the SAB 8352-5 executes instructions from the internal ROM when the PC is less than 8000H. When EA# is held on low level, the SAB 80513/8352-5 fetches all instructions from external program memory.
P0.0-P0.7	39-32	43-36	I/O	**Port 0** is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
V_{CC}	40	44	–	**Power Supply** during operation and program verification.
V_{SS}	20	22	–	**Ground** (0 V)
NC	–	1,12,23,34	–	**No Connection**

Block Diagram



Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct*)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct, A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2
MOV	direct,@R	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1

*) MOV A, ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A + DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Notes on data addressing modes:

Rn – Working register R0 – R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is + 127/– 128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex-code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A, *#data*
25	2	ADD	A, *data addr*
26	1	ADD	A, @R0
27	1	ADD	A, @R1
28	1	ADD	A, R0
29	1	ADD	A, R1
2A	1	ADD	A, R2
2B	1	ADD	A, R3
2C	1	ADD	A, R4
2D	1	ADD	A, R5
2E	1	ADD	A, R6
2F	1	ADD	A, R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A, *#data*
35	2	ADDC	A, *data addr*
36	1	ADDC	A, @R0
37	1	ADDC	A, @R1
38	1	ADDC	A, R0
39	1	ADDC	A, R1
3A	1	ADDC	A, R2
3B	1	ADDC	A, R3
3C	1	ADDC	A, R4
3D	1	ADDC	A, R5
3E	1	ADDC	A, R6
3F	1	ADDC	A, R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr, A*
43	3	ORL	*data addr, #data*
44	2	ORL	A, *#data*
45	2	ORL	A, *data addr*
46	1	ORL	A, @R0
47	1	ORL	A, @R1
48	1	ORL	A, R0
49	1	ORL	A, R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex-code	Number of bytes	Mnemonic	Operands
4A	1	ORL	A, R2
4B	1	ORL	A, R3
4C	1	ORL	A, R4
4D	1	ORL	A, R5
4E	1	ORL	A, R6
4F	1	ORL	A, R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr, A*
53	3	ANL	*data addr, #data*
54	2	ANL	A, *#data*
55	2	ANL	A, *data addr*
56	1	ANL	A, @R0
57	1	ANL	A, @R1
58	1	ANL	A, R0
59	1	ANL	A, R1
5A	1	ANL	A, R2
5B	1	ANL	A, R3
5C	1	ANL	A, R4
5D	1	ANL	A, R5
5E	1	ANL	A, R6
5F	1	ANL	A, R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr, A*
63	3	XRL	*data addr, #data*
64	2	XRL	A, *#data*
65	2	XRL	A, *data addr*
66	1	XRL	A, @R0
67	1	XRL	A, @R1
68	1	XRL	A, R0
69	1	XRL	A, R1
6A	1	XRL	A, R2
6B	1	XRL	A, R3
6C	1	XRL	A, R4
6D	1	XRL	A, R5
6E	1	XRL	A, R6
6F	1	XRL	A, R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C, *bit addr*
73	1	JMP	@A + DPTR
74	2	MOV	A, *#data*
75	3	MOV	*data addr, #data*
76	2	MOV	@R0, *#data*
77	2	MOV	@R1, *#data*
78	2	MOV	R0, *#data*
79	2	MOV	R1, *#data*
7A	2	MOV	R2, *#data*
7B	2	MOV	R3, *#data*
7C	2	MOV	R4, *#data*
7D	2	MOV	R5, *#data*
7E	2	MOV	R6, *#data*
7F	2	MOV	R7, *#data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C, *bit addr*
83	1	MOVC	A, @A + PC
84	1	DIV	AB
85	3	MOV	*data addr, data addr*
86	2	MOV	*data addr,* @R0
87	2	MOV	*data addr,* @R1
88	2	MOV	*data addr,* R0
89	2	MOV	*data addr,* R1
8A	2	MOV	*data addr,* R2
8B	2	MOV	*data addr,* R3
8C	2	MOV	*data addr,* R4
8D	2	MOV	*data addr,* R5
8E	2	MOV	*data addr,* R6
8F	2	MOV	*data addr,* R7
90	3	MOV	DPTR, *#data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr,* C
93	1	MOVC	A, @A + DPTR

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex-code	Number of bytes	Mnemonic	Operands
94	2	SUBB	A, *#data*
95	2	SUBB	A, *data addr*
96	1	SUBB	A, @R0
97	1	SUBB	A, @R1
98	1	SUBB	A, R0
99	1	SUBB	A, R1
9A	1	SUBB	A, R2
9B	1	SUBB	A, R3
9C	1	SUBB	A, R4
9D	1	SUBB	A, R5
9E	1	SUBB	A, R6
9F	1	SUBB	A, R7
A0	2	ORL	C, */bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C, *bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0, *data addr*
A7	2	MOV	@R1, *data addr*
A8	2	MOV	R0, *data addr*
A9	2	MOV	R1, *data addr*
AA	2	MOV	R2, *data addr*
AB	2	MOV	R3, *data addr*
AC	2	MOV	R4, *data addr*
AD	2	MOV	R5, *data addr*
AE	2	MOV	R6, *data addr*
AF	2	MOV	R7, *data addr*
B0	2	ANL	C, */bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,*#data, code addr*
B5	3	CJNE	A,*data addr,code addr*
B6	3	CJNE	@R0, *#data, code addr*
B7	3	CJNE	@R1, *#data, code addr*
B8	3	CJNE	R0, *#data, code addr*
B9	3	CJNE	R1, *#data, code addr*
BA	3	CJNE	R2, *#data, code addr*
BB	3	CJNE	R3, *#data, code addr*
BC	3	CJNE	R4, *#data, code addr*
BD	3	CJNE	R5, *#data, code addr*
BE	3	CJNE	R6, *#data, code addr*
BF	3	CJNE	R7, *#data, code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A, *data addr*
C6	1	XCH	A, @R0
C7	1	XCH	A, @R1
C8	1	XCH	A, R0
C9	1	XCH	A, R1
CA	1	XCH	A, R2
CB	1	XCH	A, R3
CC	1	XCH	A, R4
CD	1	XCH	A, R5
CE	1	XCH	A, R6
CF	1	XCH	A, R7
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr, code addr*
D6	1	XCHD	A, @R0
D7	1	XCHD	A, @R1
D8	2	DJNZ	R0, *code addr*
D9	2	DJNZ	R1, *code addr*
DA	2	DJNZ	R2, *code addr*
DB	2	DJNZ	R3, *code addr*
DC	2	DJNZ	R4, *code addr*
DD	2	DJNZ	R5, *code addr*

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex-code	Number of bytes	Mnemonic	Operands
DE	2	DJNZ	R6, *code addr*
DF	2	DJNZ	R7, *code addr*
E0	1	MOVX	A, @DPTR
E1	2	AJMP	code addr
E2	1	MOVX	A, @R0
E3	1	MOVX	A, @R1
E4	1	CLR	A
E5	2	MOV	A, *data addr* *)
E6	1	MOV	A, @R0
E7	1	MOV	A, @R1
E8	1	MOV	A, R0
E9	1	MOV	A, R1
EA	1	MOV	A, R2
EB	1	MOV	A, R3
EC	1	MOV	A, R4
ED	1	MOV	A, R5
EE	1	MOV	A, R6
EF	1	MOV	A, R7
F0	1	MOVX	@DPTR, A
F1	2	ACALL	code addr
F2	1	MOVX	@R0, A
F3	1	MOVX	@R1, A
F4	1	CPL	A
F5	2	MOV	*data addr*, A
F6	1	MOV	@R0, A
F7	1	MOV	@R1, A
F8	1	MOV	R0, A
F9	1	MOV	R1, A
FA	1	MOV	R2, A
FB	1	MOV	R3, A
FC	1	MOV	R4, A
FD	1	MOV	R5, A
FE	1	MOV	R6, A
FF	1	MOV	R7, A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	0 to + 70 °C
	– 40 to + 85 °C (for - T3)
Storage temperature	– 65 to + 150 °C
Voltage on any pin with respect to ground (V_{SS})	– 0.5 to + 7 V
Power dissipation	2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; T_A = – 40 to + 85 °C for T3; V_{CC} = 5 V ± 10 %; V_{SS} = 0 V

Symbol	Parameter	Limit Values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	– 0.5	0.8	V	–
V_{IH}	Input high voltage (except RST/V_{PD} and XTAL2)	2.0	V_{CC} + 0.5	V	–
V_{IH1}	Input high voltage to RST/V_{PD} for reset, XTAL2	2.5	V_{CC} + 0.5	V	XTAL1 to V_{SS}
V_{PD}	Power down voltage to RST/V_{PD}	4.5	5.5	V	V_{CC} = 0 V
V_{OL}	Output low voltage Ports 1, 2, 3	–	0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output low voltage Port 0, ALE, PSEN#	–	0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output high voltage Ports 1, 2, 3	2.4	–	V	I_{OH} = – 80 µA
V_{OH1}	Output high voltage Port 0, ALE, PSEN#	2.4	–	V	I_{OH} = – 400 µA
I_{IL}	Logical 0 input current Ports 1, 2, 3	–	– 500	µA	V_{IL} = 0.45 V
I_{IL2}	Logical 0 input current XTAL2	–	– 3.2	mA	XTAL1 = V_{SS} V_{IL} = 0.45 V
I_{IH1}	Input high current to RST/V_{PD} for reset	–	500	µA	V_{IN} = V_{CC} – 1.5V
I_{LI}	Input leakage current to port 0, EA#	–	± 10	µA	0 V < V_{IN} < V_{CC}
I_{CC}	Power supply current SAB 80513 SAB 80513-16 SAB 80513-16-T3 SAB 8352-5 SAB 8352-5-16 SAB 8352-5-16-T3	 – – – – – –	 175 175 200 200 TBD TBD	mA	all outputs disconnected
I_{PD}	Power down current	–	15	mA	V_{CC} = 0 V
C_{IO}	Capacitance of I/O buffer	–	10	pF	f_C = 1 MHz

AC Characteristics for SAB 80513/8352-5

T_A = 0 to 70 °C; T_A = – 40 to + 85 °C for T3; V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
(C_L for port 0, ALE and PSEN# outputs = 100 pF; C_L for all other outputs = 80 pF)

Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 to 12 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
t_{LHLL}	ALE pulse width	127	–	2 t_{CLCL} – 40	–	ns
t_{AVLL}	Address setup to ALE	53	–	t_{CLCL} – 30	–	ns
t_{LLAX1}	Address hold after ALE	48	–	t_{CLCL} – 35	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	4 t_{CLCL} – 100	ns
t_{LLPL}	ALE to PSEN#	58	–	t_{CLCL} – 25	–	ns
t_{PLPH}	PSEN# pulse width	215	–	3 t_{CLCL} – 35	–	ns
t_{PLIV}	PSEN# to valid instruction in	–	150	–	3 t_{CLCL} – 100	ns
t_{PXIX}	Input instruction hold after PSEN#	0	–	0	–	ns
t_{PXIZ} 1)	Input instruction float after PSEN#	–	63	–	t_{CLCL} – 20	ns
t_{PXAV} 1)	Address after PSEN#	75	–	t_{CLCL} – 8	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	5 t_{CLCL} – 115	ns
t_{AZPL}	Address float to PSEN#	0	–	0	–	ns
External Data Memory Characteristics						
t_{RLRH}	RD# pulse width	400	–	6 t_{CLCL} – 100	–	ns
t_{WLWH}	WR# pulse width	400	–	6 t_{CLCL} – 100	–	ns
t_{LLAX2}	Address hold after ALE	132	–	2 t_{CLCL} – 35	–	ns
t_{RLDV}	RD# to valid data in	–	252	–	5 t_{CLCL} – 165	ns
t_{RHDX}	Data hold after RD#	0	–	0	–	ns
t_{RHDZ}	Data float after RD#	–	55	–	2 t_{CLCL} – 70	ns
t_{LLDV}	ALE to valid data in	–	550	–	8 t_{CLCL} – 150	ns
t_{AVDV}	Address to valid data in	–	598	–	9 t_{CLCL} – 165	ns
t_{LLWL}	ALE to WR# or RD#	200	300	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
t_{AVWL}	Address to WR# or RD#	203	–	4 t_{CLCL} – 130	–	ns
t_{WHLH}	WR# or RD# high to ALE high	43	123	t_{CLCL} – 40	t_{CLCL} + 40	ns
t_{QVWX}	Data valid to WR# transition	33	–	t_{CLCL} – 50	–	ns
t_{QVWH}	Data setup before WR#	433	–	7 t_{CLCL} – 150	–	ns
t_{WHQX}	Data hold after WR#	33	–	t_{CLCL} – 50	–	ns
t_{RLAZ}	Address float after RD#	–	0	–	0	ns

1) Interfacing the SAB 80513/8352-5 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

Symbol	Parameter	Limit Values		Unit
		Variable clock Freq. = 1.2 to 12 MHz		
		min.	max.	

External Clock Drive XTAL2

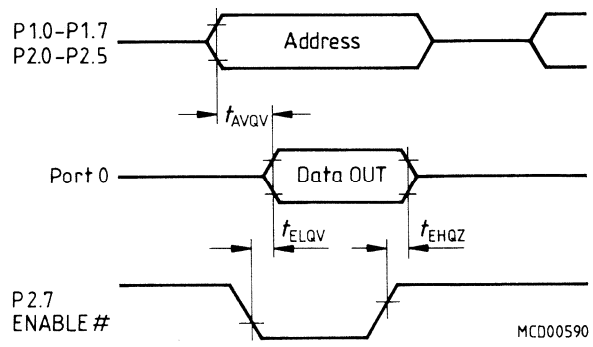
t_{CLCL}	Oscillator period	83.3	833.3	ns
t_{CHCX}	High time	20	$t_{CLCL} - t_{CLCX}$	ns
t_{CLCX}	Low time	20	$t_{CLCL} - t_{CLCX}$	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

ROM Verification Characteristics for SAB 80513/80513-16

T_A = 25 °C ± 5 °C; V_{CC} = 5 V ± 10 %; V_{SS} = 0 V

Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	$48t_{CLCL}$	ns
t_{ELQV}	ENABLE# to valid data	–	$48t_{CLCL}$	ns
t_{EHQZ}	Data float after ENABLE#	0	$48t_{CLCL}$	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification



Address:	P1.0 – P1.7	= A0 – A7	Inputs:	P2.6, PSEN#	= V_{SS}
	P2.0 – P2.5	= A8 – A13		ALE, EA#	= V_{IH}
Data:	Port 0	= D0 – D7		RST/V_{PD}	= V_{IH1}

AC Characteristics for SAB 80513-16/8352-5-16

T_A = 0 to 70 °C; T_A = – 40 to + 85 °C for T3; V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
(C_L for port 0, ALE and PSEN# outputs = 100 pF; C_L for all other outputs = 80 pF)

Symbol	Parameter	Limit Values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 to 16 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
t_{LHLL}	ALE pulse width	85	–	2 t_{CLCL} – 40	–	ns
t_{AVLL}	Address setup to ALE	33	–	t_{CLCL} – 30	–	ns
t_{LLAX1}	Address hold after ALE	28	–	t_{CLCL} – 35	–	ns
t_{LLIV}	ALE to valid instruction in	–	150	–	4 t_{CLCL} – 100	ns
t_{LLPL}	ALE to PSEN#	38	–	t_{CLCL} – 25	–	ns
t_{PLPH}	PSEN# pulse width	153	–	3 t_{CLCL} – 35	–	ns
t_{PLIV}	PSEN# to valid instruction in	–	88	–	3 t_{CLCL} – 100	ns
t_{PXIX}	Input instruction hold after PSEN#	0	–	0	–	ns
t_{PXIZ} 1)	Input instruction float after PSEN#	–	48	–	t_{CLCL} – 15	ns
t_{PXAV} 1)	Address after PSEN#	60	–	t_{CLCL} – 3	–	ns
t_{AVIV}	Address to valid instruction in	–	223	–	5 t_{CLCL} – 90	ns
t_{AZPL}	Address float to PSEN#	0	–	0	–	ns
External Data Memory Characteristics						
t_{RLRH}	RD# pulse width	275	–	6 t_{CLCL} – 100	–	ns
t_{WLWH}	WR# pulse width	275	–	6 t_{CLCL} – 100	–	ns
t_{LLAX2}	Address hold after ALE	90	–	2 t_{CLCL} – 35	–	ns
t_{RLDV}	RD# to valid data in	–	148	–	5 t_{CLCL} – 165	ns
t_{RHDX}	Data hold after RD#	0	–	0	–	ns
t_{RHDZ}	Data float after RD#	–	55	–	2 t_{CLCL} – 70	ns
t_{LLDV}	ALE to valid data in	–	350	–	8 t_{CLCL} – 150	ns
t_{AVDV}	Address to valid data in	–	398	–	9 t_{CLCL} – 165	ns
t_{LLWL}	ALE to WR# or RD#	138	238	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
t_{AVWL}	Address to WR# or RD#	120	–	4 t_{CLCL} – 130	–	ns
t_{WHLH}	WR# or RD# high to ALE high	23	103	t_{CLCL} – 40	t_{CLCL} + 40	ns
t_{QVWX}	Data valid to WR# transition	13	–	t_{CLCL} – 50	–	ns
t_{QVWH}	Data setup before WR#	288	–	7 t_{CLCL} – 150	–	ns
t_{WHQX}	Data hold after WR#	13	–	t_{CLCL} – 50	–	ns
t_{RLAZ}	Address float after RD#	–	0	–	0	ns

1) Interfacing the SAB 80513-16/8352-5-16 to devices with float times up to 55 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

Symbol	Parameter	Limit Values		Unit
		Variable clock Freq. = 1.2 to 16 MHz		
		min.	max.	

External Clock Drive XTAL2

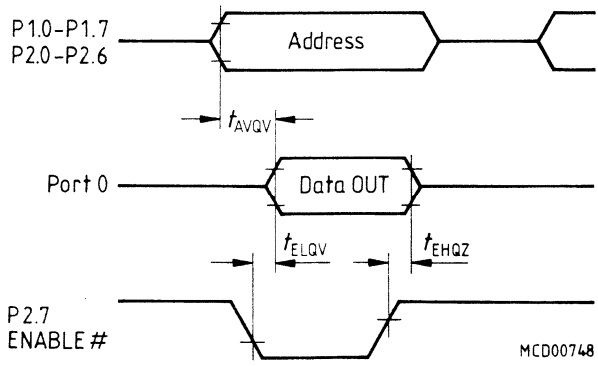
t_{CLCL}	Oscillator period	62.5	833.3	ns
t_{CHCX}	High time	15	$t_{CLCL} - t_{CLCX}$	ns
t_{CLCX}	Low time	15	$t_{CLCL} - t_{CHCX}$	ns
t_{CLCH}	Rise time	–	15	ns
t_{CHCL}	Fall time	–	15	ns

ROM Verification Characteristics for SAB 80513/80513-16

T_A = 25 °C ± 5 °C; V_{CC} = 5 V ± 10 %; V_{SS} = 0 V

Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	$48t_{CLCL}$	ns
t_{ELQV}	ENABLE# to valid data	–	$48t_{CLCL}$	ns
t_{EHQZ}	Data float after ENABLE#	0	$48t_{CLCL}$	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

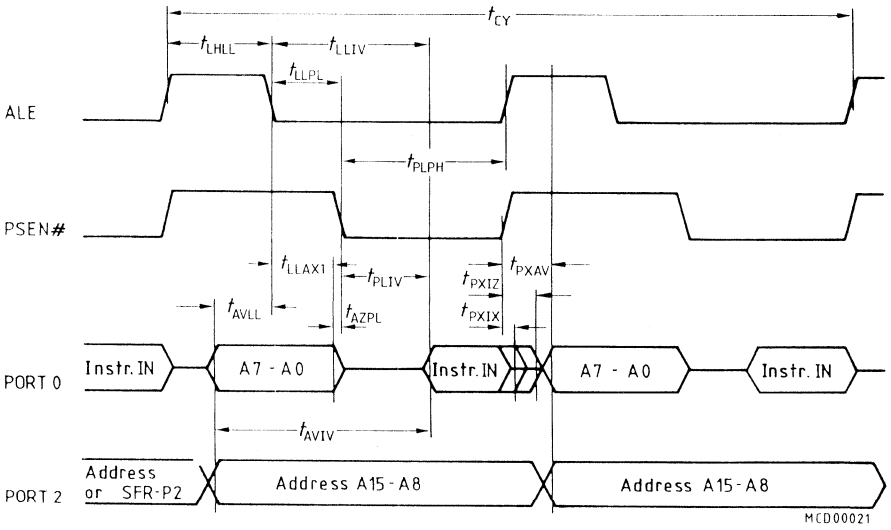
ROM Verification



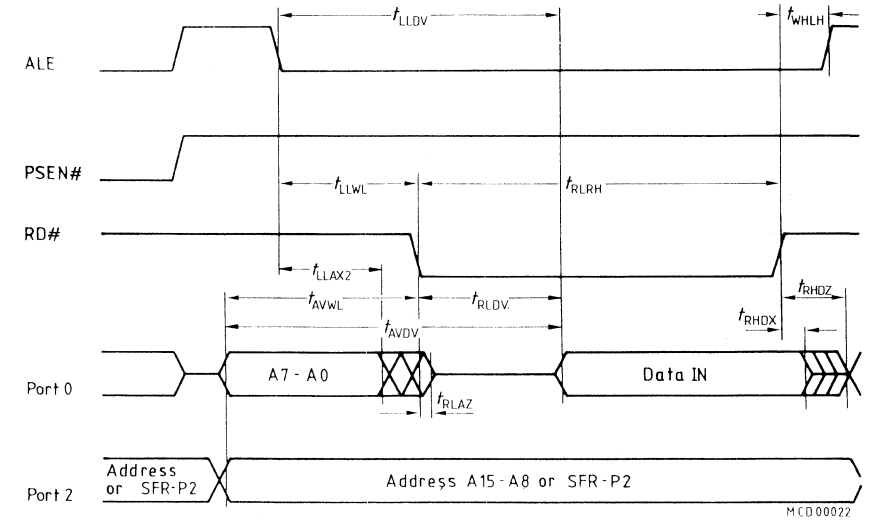
Address:	P1.0 – P1.7	= A0 – A7	Inputs:	P2.6, PSEN#	= V_{SS}
	P2.0 – P2.6	= A8 – A14		ALE, EA#	= V_{IH}
Data:	Port 0	= D0 – D7		RST/V_{PD}	= V_{IH1}

Waveforms

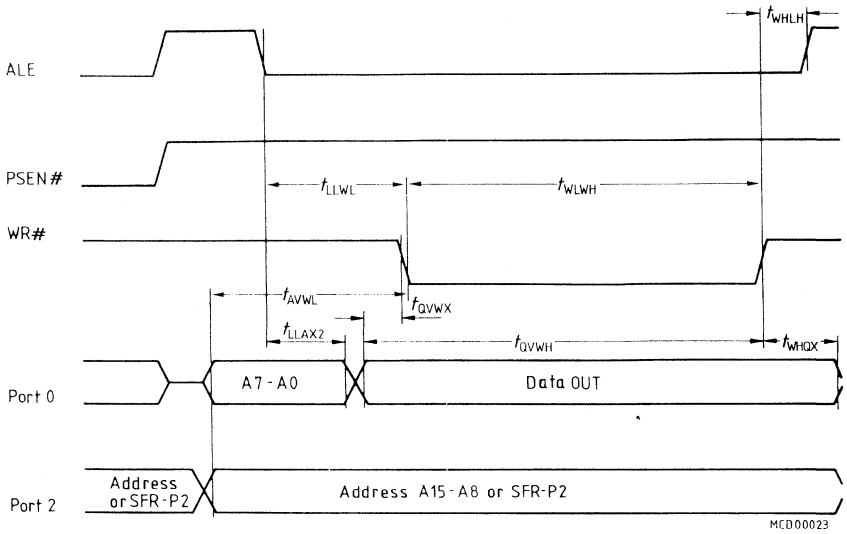
Program Memory Read Cycle



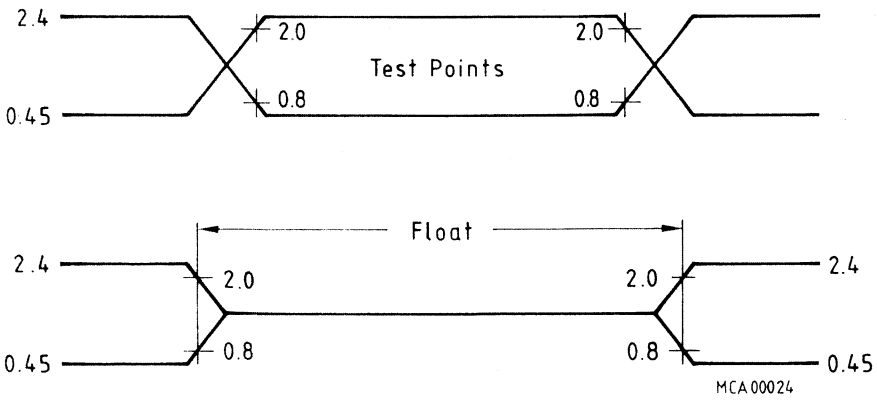
Data Memory Read Cycle



Data Memory Write Cycle

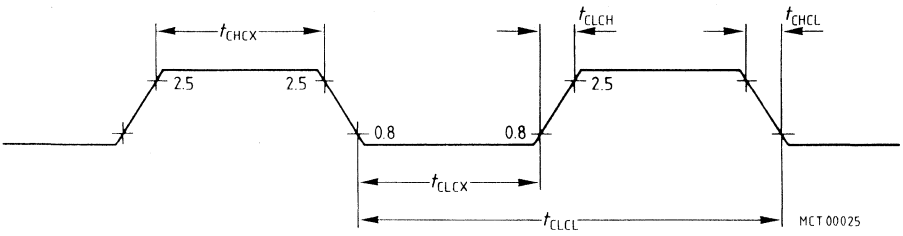


AC Testing Input, Output, Float Waveforms

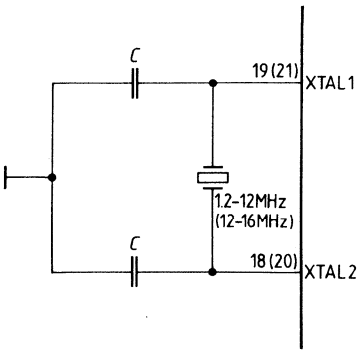


AC testing inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2 mA or sources 400 µA at voltage test levels.

External Clock Cycle



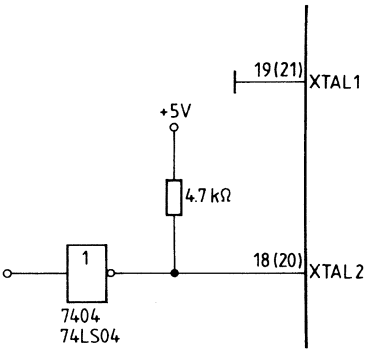
Recommended Oscillator Circuits



$C = 30\,pF \pm 10\,pF$

Crystal Oscillator Mode

Pin numbers in (...) are for PL-CC-44 package



Driving from External Source MCS00747

SIEMENS

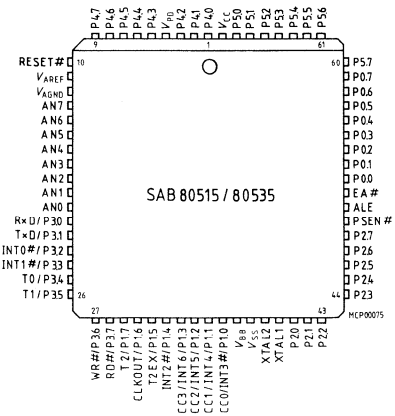
8-Bit Single Chip Microcontroller — SAB 80515/80535

Preliminary

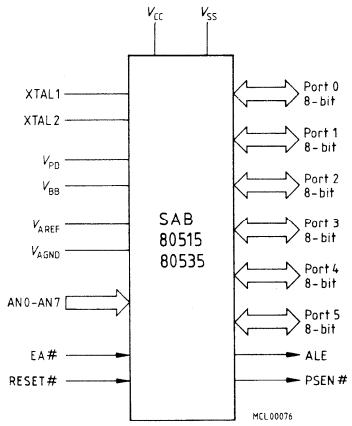
SAB 80515-N Microcontroller with factory mask-programmable ROM
SAB 80535-N Microcontroller for external ROM

- 8K × 8 ROM (SAB 80515 only)
- 256 × 8 RAM
- Six 8-bit I/O ports, one 8-bit input port for analog signals
- Three 16-bit timer/counters
- Highly flexible reload, capture, compare capabilities
- Full-duplex serial channel
- Twelve interrupt vectors, four priority levels
- 8-bit A/D converter with eight multiplexed inputs and programmable internal reference voltages
- 16-bit watchdog timer
- V_{PD} provides standby current for 40 bytes of RAM
- Boolean processor
- 256 bit-addressable locations
- Most instructions execute in 1 µs
- 4 µs multiply and divide
- External memory expandable up to 128 Kbyte
- Backwardly compatible with SAB 8051
- 68-pin plastic leaded chip carrier package (PL-CC-68)

Pin Configuration (PL-CC-68)



Logic Symbol



The SAB 80515/80535 is a powerful member of the Siemens SAB 8051 family of 8-bit microcontrollers. It is fabricated in + 5 V N-channel, silicon-gate Siemens MYMOS technology. The SAB 80515/80535 is a stand-alone, high-performance single-chip microcontroller based on the SAB 8051 architecture. While maintaining all the SAB 8051 operating characteristics, the SAB 80515/80535 incorporates several enhancements which significantly increase design flexibility and overall system performance.
The SAB 80535 is identical with the SAB 80515 except that it lacks the on-chip program memory. The SAB 80515/80535 is supplied in a 68-pin plastic leaded chip carrier package (PL-CC-68).

Ordering Information

Type	Ordering code	Package	Description
			8-bit single-chip microcontroller
SAB 80515-N	Q 67120-C211	PL-CC-68	with mask-programmable ROM
SAB 80535-N	Q 67120-C241	PL-CC-68	for external memory

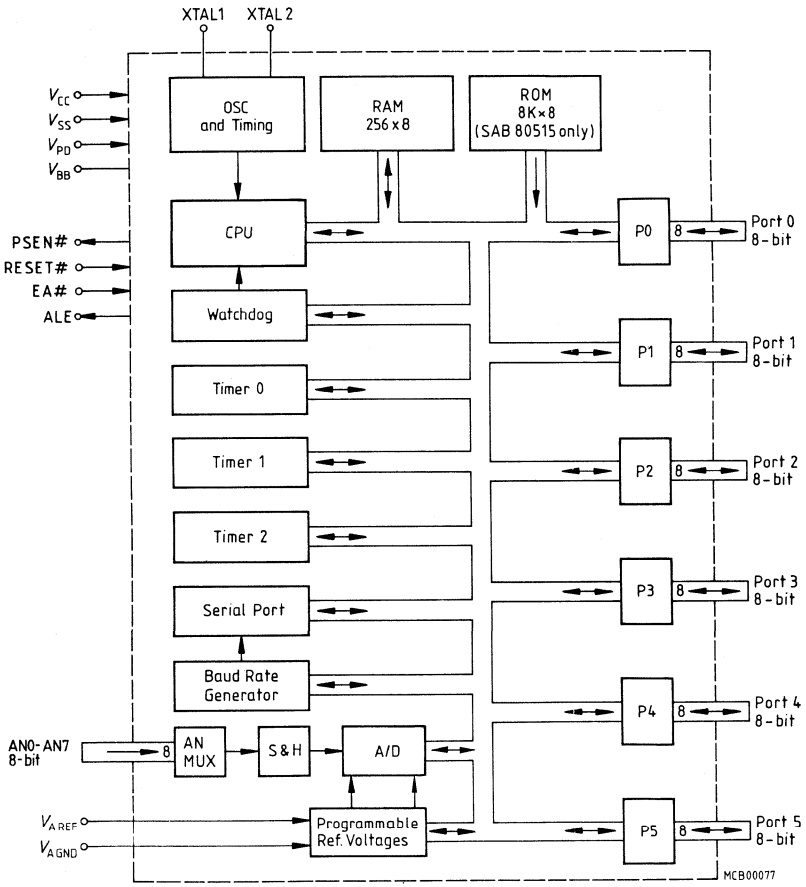
Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	I/O	Port 4 is an 8-bit quasi-bidirectional I/O port. Port 4 can sink/source 4 LS-TTL loads.
V_{PD}	4		Power down supply. If V_{PD} is held within its specs while V_{CC} drops below specs, V_{PD} will provide standby power to 40 byte of the internal RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
$\overline{\text{RESET}}$	10	I	A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80515. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	11		Reference voltage for the A/D converter
V_{AGND}	12		Reference ground for the A/D converter
AN7-AN0	13-20	I	Multiplexed analog inputs
P3.0-P3.7	21-28	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source 4 LS-TTL loads. The secondary functions are assigned to the pins of port 3, as follows: – RxD (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – TxD (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{\text{INT0}}$ (P3.2): interrupt 0 input / timer 0 gate control input – $\overline{\text{INT1}}$ (P3.3): interrupt 1 input / timer 1 gate control input – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{\text{WR}}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{\text{RD}}$ (P3.7): the read control signal enables the external data memory to port 0
P1.7-P1.0	29-36	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. It also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch must be programmed to a one (1) for that function to operate (except when used for the compare functions). Port 1 can sink/source 4 LS-TTL loads. The secondary functions are assigned to the port 1 pins, as follows: – $\overline{\text{INT3}}$/CC0 (P1.0): interrupt 3 input/compare 0 output/ capture 0 input – INT4/CC1 (P1.1): interrupt 4 input/compare 1 output/ capture 1 input – INT5/CC2 (P1.2): interrupt 5 input/compare 2 output/ capture 2 input – INT6/CC3 (P1.3): interrupt 6 input/compare 3 output/ capture 3 input

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P1.7-P1.0 (cont'd)			– $\overline{INT2}$ (P1.4): interrupt 2 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input
V_{BB}	37		Substrate pin. Must be connected to V_{SS} through a capacitor (47 to 100 nF) for proper operation of the A/D converter.
XTAL2	39		XTAL2 is the output from the oscillator's amplifier.Input to the internal timing circuitry. A crystal, ceramic resonator, or external source can be used.
XTAL1	40		XTAL1 is the input to the oscillator's high gain amplifier. Required when a crystal or ceramic resonator is used. Connect to V_{SS} when external source is used on XTAL2.
P2.0-P2.7	41-48	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source 4 LS-TTL loads.
$\overline{PSEN}$	49	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during internal program execution.
ALE	50	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{EA}$	51	I	When held at a TTL high level, the SAB 80515 executes instructions from the internal ROM when the PC is less than 8192. When held at a TTL low level, the SAB 80515 fetches all instructions from external program memory. For the SAB 80535 this pin must be tied low.
P0.0-P0.7	52-59	I/O	Port 0 is an 8-bit open-drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source 8 LS-TTL loads.
P5.7-P5.0	60-67	I/O	Port 5 is an 8-bit quasi-bidirectional I/O port. Port 5 can sink/source 4 LS-TTL loads.
V_{CC}	68		POWER SUPPLY (+ 5 V power supply during normal operation and program verification)
V_{SS}	38		GROUND (0 V)

Figure 1
Block Diagram



Functional Description

The members of the SAB 80515 family of microcontrollers are:

- SAB 80515: Microcontroller, designed in Siemens MYMOS technology, with 8 Kbyte factory mask-programmable ROM
- SAB 80535: ROM-less version of the SAB 80515
- SAB 80C515: Microcontroller, designed in Siemens ACMOS technology, with 8 Kbyte factory mask-programmable ROM
- SAB 80C535: ROM-less version of the SAB 80C515
- SAB 80515K: Special ROM-less version of the SAB 80515 with an additional interface for program memory accesses. An external ROM that is accessed via this interface substitutes the SAB 80515's internal ROM.

The SAB 80535 is identical to the SAB 80515, except that it lacks the on-chip ROM. In this data sheet the term "SAB 80515" is used to refer to both the SAB 80515 and SAB 80535, unless otherwise noted.

Principles of Architecture

The architecture of the SAB 80515 is based on the SAB 8051 microcontroller family. The following features of the SAB 80515 are fully compatible with the SAB 8051 features:

- Instruction set
- External memory expansion interface (port 0 and port 2)
- Full-duplex serial port
- Timer/counter 0 and 1
- Alternate functions on port 3
- The lower 128 bytes of internal RAM and the lower 4 Kbytes of internal ROM

The SAB 80515 additionally contains 128 bytes of internal RAM and 4 Kbytes of internal ROM, which results in a total of 256 bytes of RAM and 8 Kbytes of ROM on chip. The SAB 80515 has a new 16-bit timer/counter with a 2:1 prescaler, reload mode, compare and capture capability. It also contains a 16-bit watchdog timer, an 8-bit A/D converter with programmable reference voltages, two additional quasi-bidirectional 8-bit ports, one 8-bit input port for analog signals, and a programmable clock output ($f_{OSC}/12$). Furthermore, the SAB 80515 has a powerful interrupt structure with 12 vectors and 4 programmable priority levels.
Figure 1 shows a block diagram of the SAB 80515.

CPU

The SAB 80515 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1.0 µs.

Memory Organization

The SAB 80515 manipulates operands in the four memory address spaces described in the following. (Figure 2 illustrates the memory address spaces of the SAB 80515).

Program memory

The SAB 80515 has 8 Kbyte of on-chip ROM, while the SAB 80535 has no internal ROM. The program memory can be externally expanded up to 64 Kbytes. If the $\overline{EA}$ pin is held high, the SAB 80515 executes out of internal ROM unless the address exceeds 1FFFH. Locations 2000H through 0FFFFH are then fetched from the external program memory. If the $\overline{EA}$ pin is held low, the SAB 80515 fetches all instructions from the external program memory. Since the SAB 80535 has no internal ROM, pin $\overline{EA}$ must be tied low when using this component.

Data Memory

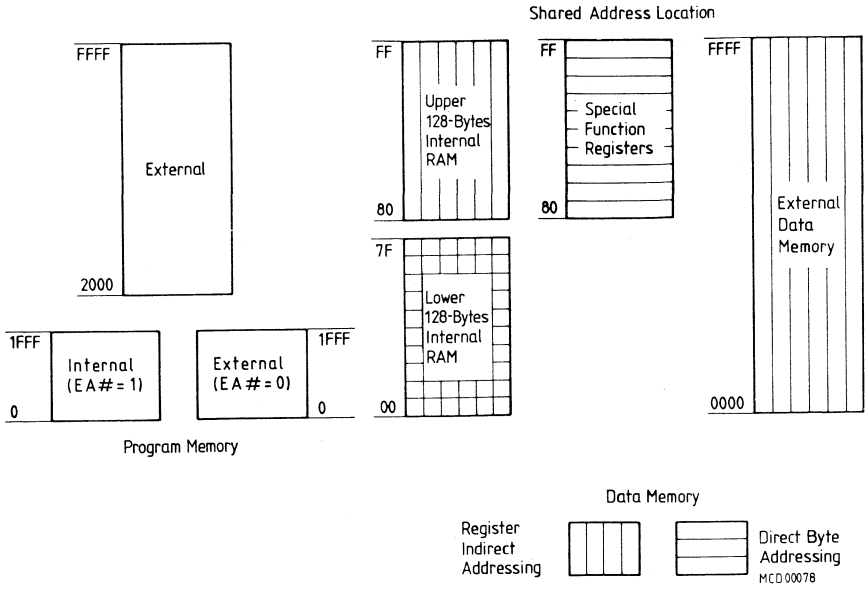
The data memory address space consists of an internal and an external memory space. The internal data memory is divided into three physically separate and distinct blocks: the lower 128 bytes of RAM, the upper 128 bytes of RAM, and the 128-byte special function register (SFR) area. While the upper 128 bytes of data memory and the SFR area share the same address locations, they are accessed through different addressing modes. The lower 128 bytes of data memory can be accessed through direct or register indirect addressing; the upper 128 bytes of RAM can be accessed through register indirect addressing; the special function registers are accessible through direct addressing.
Four 8-register banks, each bank consisting of eight 8-bit multi-purpose registers, occupy locations 0 through 1FH in the lower RAM area. The next 16 bytes, locations 20H through 2FH, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal data memory address space, and the stack depth can be expanded up to 256 bytes.
The external data memory can be expanded up to 64 Kbytes and can be accessed by instructions that use a 16-bit or an 8-bit address.

All registers, except the program counter and the four 8-register banks, reside in the special function register area. The 41 special function registers (SFR's) include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripheral functions. There are also 128 directly addressable bits within the SFR area. The special function registers are listed in the following table:

Symbol	Name	Address
* P0	Port 0	80H
SP	Stack pointer	81H
DPL	Data pointer, low byte	82H
DPH	Data pointer, high byte	83H
PCON	Power control register	87H
* TCON	Timer control register	88H
TMOD	Timer mode register	89H
TL0	Timer 0, low byte	8AH
TL1	Timer 1, low byte	8BH
TH0	Timer 0, high byte	8CH
TH1	Timer 1, high byte	8DH
* P1	Port 1	90H
* SCON	Serial port control register	98H
SBUF	Serial port buffer register	99H
* P2	Port 2	0A0H
* IEN0	Interrupt enable register 0	0A8H
IP0	Interrupt priority register 0	0A9H
* P3	Port 3	0B0H
* IEN1	Interrupt enable register 1	0B8H
IP1	Interrupt priority register 1	0B9H
* IRCON	Interrupt request control register	0C0H
CCEN	Compare/capture enable register	0C1H
CCL1	Compare/capture register 1, low byte	0C2H
CCH1	Compare/capture register 1, high byte	0C3H
CCL2	Compare/capture register 2, low byte	0C4H
CCH2	Compare/capture register 2, high byte	0C5H
CCL3	Compare/capture register 3, low byte	0C6H
CCH3	Compare/capture register 3, high byte	0C7H
* T2CON	Timer 2 control register	0C8H
CRCL	Compare/reload/capture register, low byte	0CAH
CRCH	Compare/reload/capture register, high byte	0CBH
TL2	Timer 2, low byte	0CCH
TH2	Timer 2, high byte	0CDH
* PSW	Program status word register	0D0H
* ADCON	A/D-converter control register	0D8H
ADDAT	A/D-converter data register	0D9H
DAPR	D/A-converter program register	0DAH
* ACC	Accumulator	0E0H
* P4	Port 4	0E8H
* B	B register	0F0H
* P5	Port 5	0F8H

The SFR's marked with an asterisk (*) are both bit and byte-addressable.

Figure 2
Memory Address Spaces



I/O Ports

The SAB 80515 has six 8-bit I/O ports and one 8-bit input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pull-up resistors. That means, when configured as inputs, ports 1 to 5 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.
Ports 1 and 3 are provided for several alternate functions, as listed below:

Port	Symbol	Function
P1.0	$\overline{\text{INT3}}$/CC0	External interrupt 3 input, compare 0 output, capture 0 input
P1.1	INT4/CC1	External interrupt 4 input, compare 1 output, capture 1 input
P1.2	INT5/CC2	External interrupt 5 input, compare 2 output, capture 2 input
P1.3	$\overline{\text{INT6}}$/CC3	External interrupt 6 input, compare 3 output, capture 3 input
P1.4	INT2	External interrupt 2 input
P1.5	T2EX	Timer 2 external reload trigger input
P1.6	CLKOUT	System clock output
P1.7	T2	Timer 2 external counter input
P3.0	RXD	Serial port's receiver data input (asynchronous) or data input/output (synchronous)
P3.1	$\overline{\text{TXD}}$	Serial port's transmitter data output (asynchronous) or clock output (synchronous)
P3.2	$\overline{\text{INT0}}$	External interrupt 0 input, timer 0 gate control
P3.3	$\overline{\text{INT1}}$	External interrupt 1 input, timer 1 gate control
P3.4	T0	Timer 0 external counter input
P3.5	$\overline{\text{T1}}$	Timer 1 external counter input
P3.6	$\overline{\text{WR}}$	External data memory write strobe
P3.7	$\overline{\text{RD}}$	External data memory read strobe

The input port AN0-AN7 is used for analog input signals to the A/D converter.

Timer/Counters

The SAB 80515 contains three 16-bit timer/counters which are useful in many applications for timing and counting. The input clock for each timer/counter is 1/12 of the oscillator frequency in the timer operation or can be taken from an external clock source for the counter operation (maximum count rate is 1/24 of the oscillator frequency).

Timer/counter 0 and 1

These timer/counters can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto-reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; timer/counter 1 in this mode holds its count.

External inputs $\overline{INT0}$ and $\overline{INT1}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

Timer/counter 2

Timer/counter 2 of the SAB 80515 is a 16-bit timer/counter with several additional features. It offers a 2:1 prescaler, a selectable gate function, and compare, capture and reload functions. Corresponding to the 16-bit timer register there are four 16-bit capture/compare registers, one of them can be used to perform a 16-bit reload on a timer overflow or external event. Each of these registers corresponds to a pin of port 1 for capture input/compare output.

Figure 3 shows a block diagram of the timer/counter 2.

– Reload

A 16-bit reload can be performed with the 16-bit CRC register, which is a concatenation of the 8-bit registers CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer 2 overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

– Capture

This feature permits saving the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value in timer 2 registers into a dedicated capture register:

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

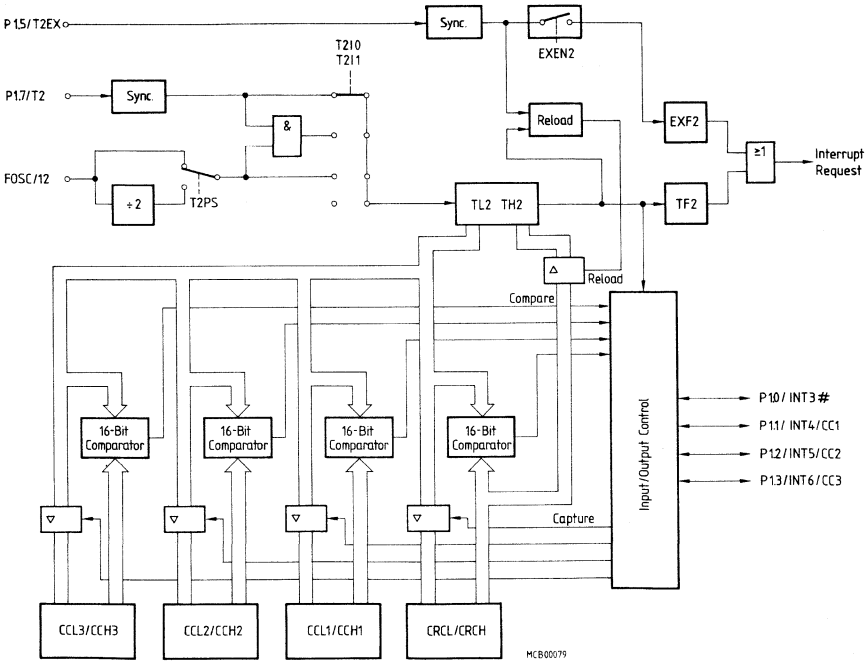
– Compare

In the compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 registers. If the count value in the timer 2 registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to a low level when timer 2 overflows.

Mode 1: The transition of the output signal can be determined by software. A timer 2 overflow causes no output change.

Figure 3
Block Diagram of Timer/Counter 2



Serial Port

The serial port of the SAB 80515 enables full duplex communication between microcontrollers or between microcontroller and peripheral devices. The serial port can operate in 4 modes:

Mode 0: Shift register mode. Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 10 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). The baud rate is variable.

Mode 2: 11 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Mode 3 is identical to mode 2 except for the baud rate. The baud rate in mode 3 is variable.

The variable baud rates in modes 1 and 3 can be generated by timer 1 or an internal baud rate generator.

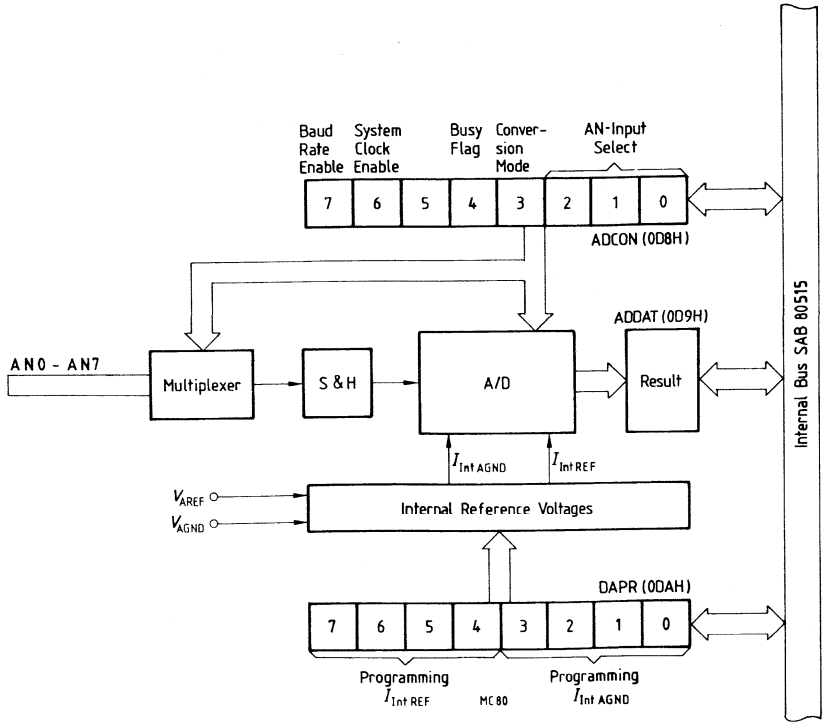
A/D Converter

The 8-bit A/D converter of the SAB 80515 has eight multiplexed analog inputs (Port 6) and uses the successive approximation method.
It takes 5 machine cycles to sample an analog signal (during this sample time the input signal should be held constant); the total conversion time (including sample time) is 15 machine cycles (15 µs at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous; at the end of a conversion an interrupt can be generated.

A unique feature is the capability of internal reference voltage programming. The internal reference voltages $V_{IntAREF}$ and $V_{IntAGND}$ for the A/D converter both are programmable to one of 16 steps with respect to the external reference voltages. This feature permits a conversion with a smaller internal reference voltage range to gain a higher resolution. In addition, the internal reference voltages can easily be adapted by software to the desired analog input voltage range.

Figure 4 shows a block diagram of the A/D converter.

Figure 4
Block Diagram of the A/D Converter



Interrupt Structure

The SAB 80515 has 12 interrupt vectors with the following vector addresses and request flags:

Table 2
Interrupt Sources and Vectors

Source (request flags)	Vector	Vector address
IE0	External interrupt 0	0003H
TF0	Timer 0 interrupt	000BH
IE1	External interrupt 1	0013H
TF1	Timer 1 interrupt	001BH
RI + TI	Serial port interrupt	0023H
TF2 + EXF2	Timer 2 interrupt	002BH
IADC	A/D converter interrupt	0043H
IEX2	External interrupt 2	004BH
IEX3	External interrupt 3	0053H
IEX4	External interrupt 4	005BH
IEX5	External interrupt 5	0063H
IEX6	External interrupt 6	006BH

Each interrupt vector can be individually enabled/disabled. The minimum response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles.

Figure 5 shows the interrupt request sources.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 3 to 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs. Each pair can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1. Figure 6 shows the priority level structure.

Figure 5
Interrupt Request Sources

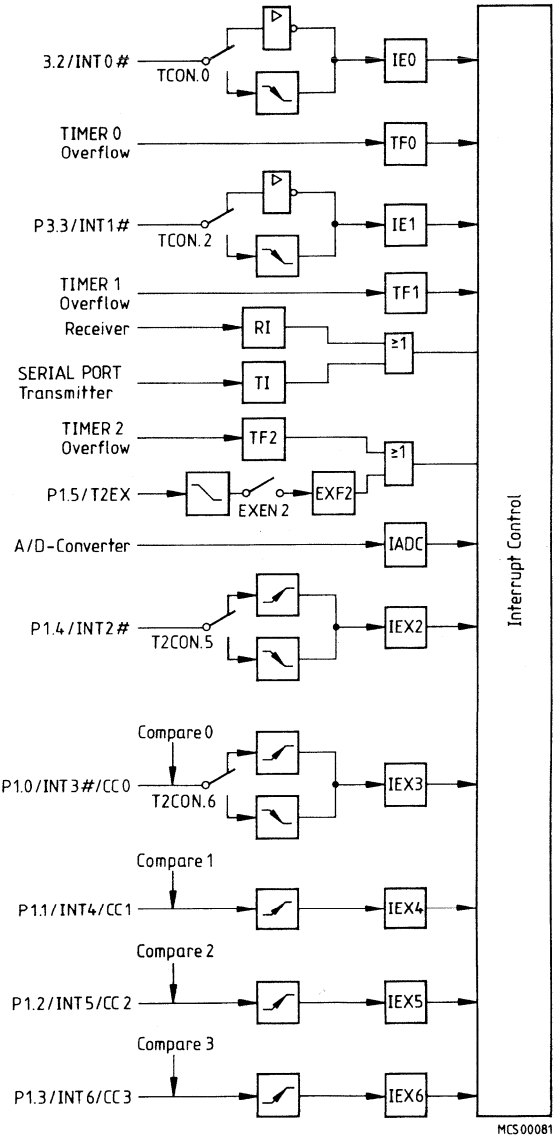
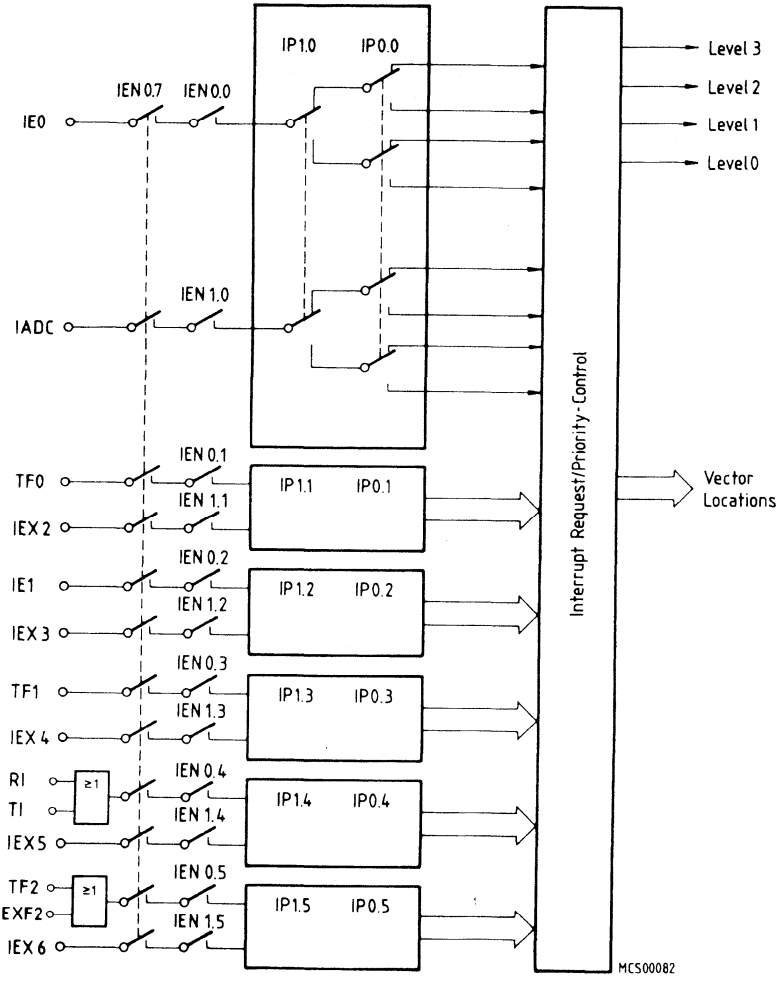


Figure 6
Priority Level Structure



Watchdog Timer

This feature is provided as a means of graceful recovery from a software upset. After an external reset, the watchdog timer is cleared and stopped. It can be started and cleared by software, but it cannot be stopped. If the software fails to clear the watchdog timer at least every 65532 machine cycles (about 65 ms if a 12 MHz oscillator frequency is used), an internal hardware reset will be initiated.

The reset cause (external reset or reset caused by the watchdog) can be examined by software. To clear the watchdog, two bits in two different special function registers must be set by two consecutive instructions (bits IEN0.6 and IEN1.6). This is done to prevent the watchdog from being cleared by unexpected opcodes.

Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A@Ri	AND indirect RAM to accumulator	1	1
ANL	A#data	AND immediate data to accumulator	2	1
ANL	direct, A	AND accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct, A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct, A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct*)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2
MOV	direct,@R	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direkct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOC	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Notes on data addressing modes:

Rn – Working register R0 – R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is + 127/– 128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr,code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr,code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,*#data*
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr,code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,*#data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr,#data*
44	2	ORL	A,*#data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr,#data*
54	2	ANL	A,*#data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr,#data*
64	2	XRL	A,*#data*
65	2	XRL	A,*data addr*

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
66	1	XRL	A,@R0
67	1	XRL	A,@R1
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr*,*data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*,R2
8B	2	MOV	*data addr*,R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data*,*code addr*
B5	3	CJNE	A,*data addr*,*code addr*
B6	3	CJNE	@R0,#*data*,*code addr*
B7	3	CJNE	@R1,#*data*,*code addr*
B8	3	CJNE	R0,#*data*,*code addr*
B9	3	CJNE	R1,#*data*,*code addr*
BA	3	CJNE	R2,#*data*,*code addr*
BB	3	CJNE	R3,#*data*,*code addr*
BC	3	CJNE	R4,#*data*,*code addr*
BD	3	CJNE	R5,#*data*,*code addr*
BE	3	CJNE	R6,#*data*,*code addr*
BF	3	CJNE	R7,#*data*,*code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr**)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr*,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	– 0 to + 70 °C
Storage temperature	– 65 to + 150 °C
Voltage on any pin with respect to ground (V_{SS})	– 0.5 to + 7 V
Power Dissipation	2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V; T_A = – 0 to + 70 °C

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Input low voltage	V_{IL}	– 0.5	0.8	V	–
Input high voltage (except RESET and XTAL2)	V_{IH}	2.0	V_{CC} + 0.5	V	–
Input high voltage to XTAL2	V_{IH1}	2.5	V_{CC} + 0.5	V	XTAL 1 to V_{SS}
Input high voltage to RESET	V_{IH2}	3.0	–	V	–
Power-down voltage	V_{PD}	3	5.5	V	V_{CC} = 0 V
Output low voltage, ports 1, 2, 3, 4, 5	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Output low voltage port 0, ALE, PSEN	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltage, ports 1, 2, 3, 4, 5	V_{OH}	2.4	–	V	I_{OH} = – 80 µA
Output high voltage port 0, ALE, PSEN	V_{OH1}	2.4	–	V	I_{OH} = – 400 µA
Logic 0 input current ports 1, 2, 3, 4, 5	I_{IL}	–	– 800	µA	V_{IL} = 0.45 V
Logic 0 input current XTAL2	I_{IL2}	–	– 2.5	mA	XTAL1 = V_{SS} V_{IL} = 0.45 V
Input low current to RESET for reset	I_{IL3}	–	– 500	µA	V_{IL} = 0.45 V
Input leakage current to port 0, EA, AN0 – AN7	I_{LI}	–	± 1	µA	0 V < V_{IN} < V_{CC}
Power supply current SAB 80515/80535	I_{CC}	–	210	mA	All outputs disconnected
Power- down current	I_{PD}	–	3		V_{CC} = 0 V
Capacitance of I/O buffer	C_{IO}	–	10	pF	f_c = 1 MHz

[1]) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1, 3, 4, 5. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-0 transcitions during bus operation.

A/D Converter Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V; V_{AREF} = V_{CC} ± 5%; V_{AGND} = V_{SS} ± 0.2 V; $V_{IntAREF} - V_{IntAGND} \geq 1$ V; T_A = 0 to +70 °C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Analog input voltage	V_{AINPUT}	V_{AGND}- 0.2	–	V_{AREF+} 0.2	V	–
Analog input capacitance	C_I	–	25	–	pF	2)
Load time	t_L	–	–	2 t_{CY}	µs	–
Sample time (incl. load time)	t_S	–	–	5 t_{CY}	µs	–
Conversion time (including sample time)	t_C	–	–	15 t_{CY}	µs	–
Differential non-linearity	DNLE	–	± 1/2	± 1	LSB	$V_{IntAREF}$ =
Integral non-linearity	INLE	–	± 1/2	± 1	LSB	V_{AREF} = V_{CC}
Offset error			± 1/2	± 1	LSB	$V_{IntAGND}$ =
Gain error			± 1/2	± 1	LSB	V_{AGND} = V_{SS}
Total unadjusted error	TUE		± 1	± 2	LSB	2)
V_{AREF} supply current	I_{REF}	–	–	5	mA	3)
Internal reference error	$V_{IntREFERR}$	–	± 5	± 15	mV	3)

2) The internal resistance of the analog source must be low enough to assure full loading of the sample capacitance (C_I) during load time (t_L). After charging of the internal capacitance (C_I) in the load time (t_L) the analog input must be held constant for the rest of the sample time (t_S).

3) The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

A/D Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V;
T_A = 0 to + 70 °C
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

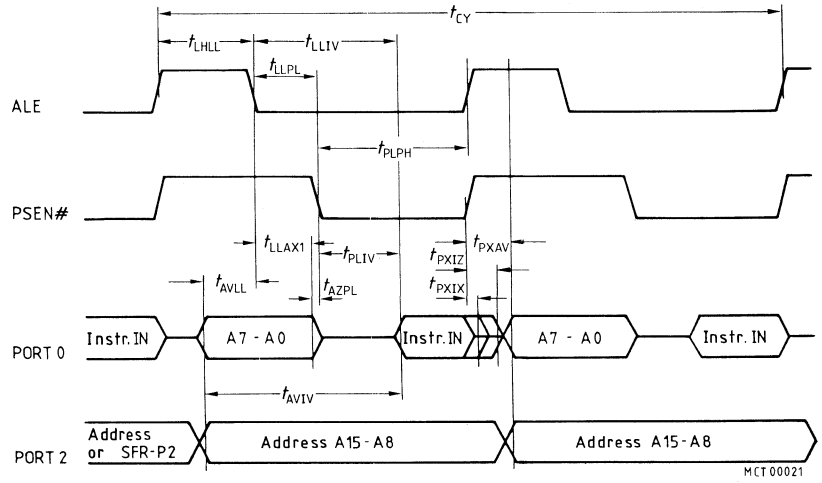
Parameter	Symbol	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
Cycle time	t_{CY}	1000	–	$12t_{CLCL}$	–	ns
ALE pulse width	t_{LHLL}	127	–	$2t_{CLCL}-40$	–	ns
Address setup to ALE	t_{AVLL}	53	–	$t_{CLCL}-30$	–	ns
Address hold after ALE	t_{LLAX1}	48	–	$t_{CLCL}-35$	–	ns
ALE to valid instruction in	t_{LLIV}	–	233	–	$4t_{CLCL}-100$	ns
ALE to $\overline{PSEN}$	t_{LLPL}	58	–	$t_{CLCL}-25$	–	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	215	–	$3t_{CLCL}-35$	–	ns
$\overline{PSEN}$ to valid instruction in	t_{PLIV}	–	150	–	$3t_{CLCL}-100$	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}*)	–	63	–	$t_{CLCL}-20$	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	75	–	$t_{CLCL}-8$	–	ns
Address to valid instruction in	t_{AVIV}	–	302	–	$5t_{CLCL}-115$	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the SAB 805156 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

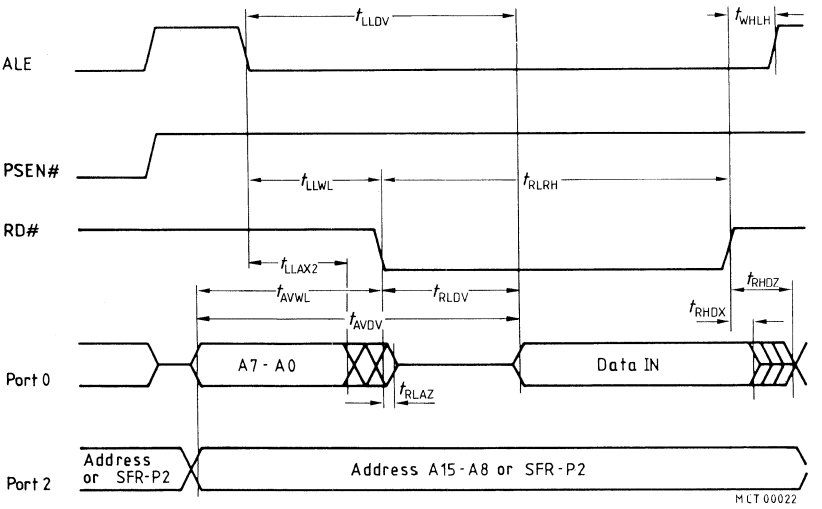
External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 1,2 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	400	–	$6t_{CLCL}-100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	$6t_{CLCL}-100$	–	ns
Address hold after ALE	t_{LLAX2}	132	–	$2t_{CLCL}-35$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	$5t_{CLCL}-165$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	$2t_{CLCL}-70$	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8t_{CLCL}-150$	ns
Address to valid data in	t_{AVDV}	–	585	–	$9t_{CLCL}-165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
Address to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203	–	$4t_{CLCL}-130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	$t_{CLCL}-50$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	–	$7t_{CLCL}-150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	$t_{CLCL}-50$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

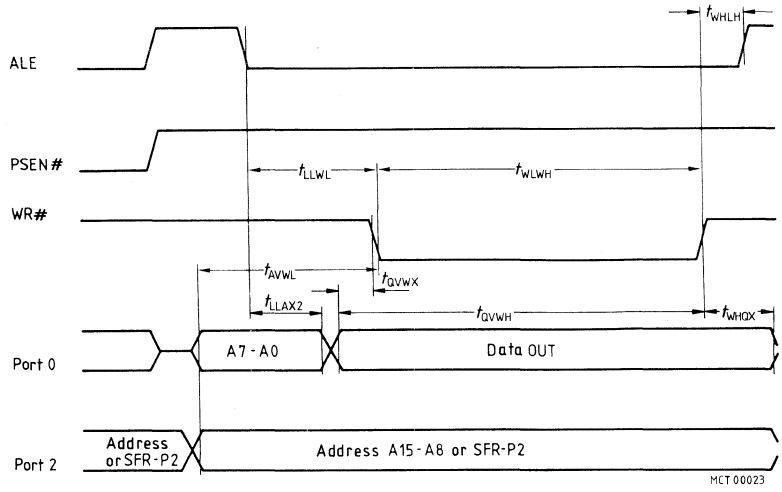
Program Memory Read Cycle



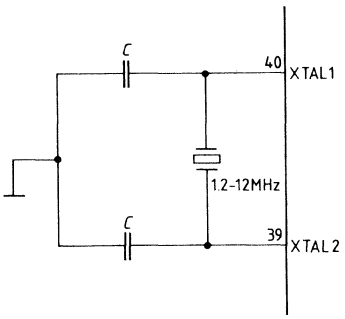
Data Memory Read Cycle



Data Memory Write Cycle

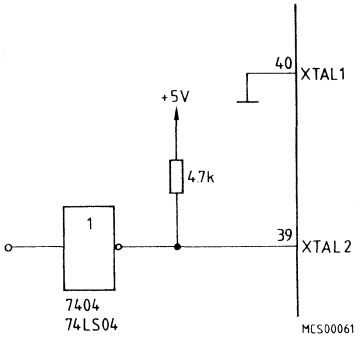


Recommended Oscillator Circuits



$C = 30\,pF \pm 10\,pF$

Crystal Oscillator Mode

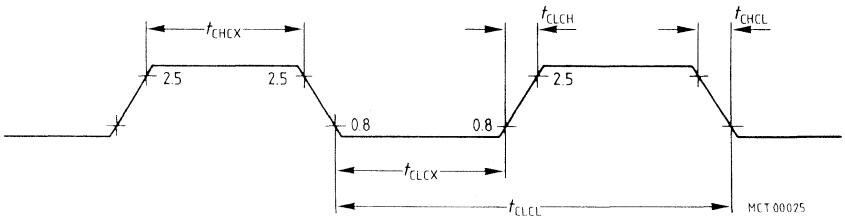


Driving from External Source

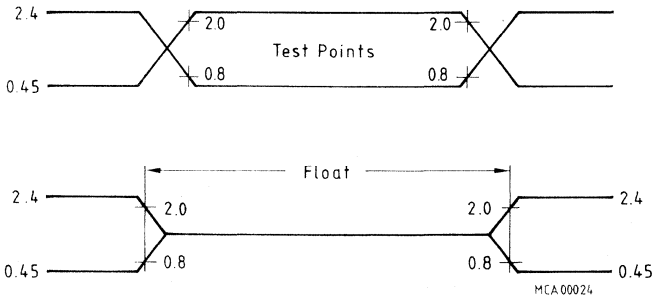
External Clock Drive XTAL2

Parameter	Symbol	Limit Values		Unit
		Variable clock Freq = 1.2 MHz to 16 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	83.3	833.3	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	15	ns
Fall time	t_{CHCL}	–	15	ns

External Clock Cycle



A.C. Testing Input, Output, Float Waveforms

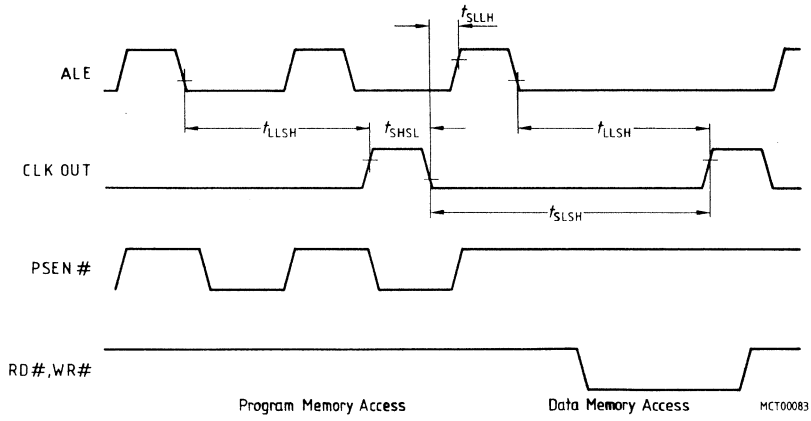


A.C. testing inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels.

System Clock Timing

Parameter	Symbol	Limit Values				Unit
		12 MHz cock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
ALE to CLKOUT	t_{LLSH}	543	–	$7t_{CLCL}-40$	–	ns
CLKOUT high time	t_{SHSL}	127	–	$2t_{CLCL}-40$	–	ns
CLKOUT low time	t_{SLSH}	793	–	$10t_{CLCL}-40$	–	ns
CLKOUT low to ALE high	t_{SLLH}	43	123	$t_{CLCL}-40$	$t_{CLCL}+40$	ns

System Clock Timing

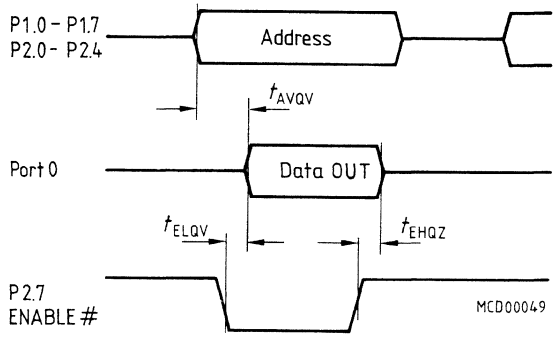


ROM Verification Characteristics

T_A = 25 °C ± °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	48 t_{CLCL}	ns
ENABLE to valid data	t_{ELQV}	–	48 t_{CLCL}	ns
Data float after ENABLE	t_{EHQZ}	0	48 t_{CLCL}	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz

ROM Verification



Address: P1.0-P1.7 = A0-A7
P2.0-P2.4 = A8-A12

Data: Port 0 = D0-D7

Inputs: P2.5-P2.6, $\overline{PSEN}$ = V_{SS}
ALE, $\overline{EA}$ = V_{IH}
RESET = V_{IL}

SIEMENS

8-Bit Single Chip Microcontroller — SAB 80515/80535 Ext. Temp.

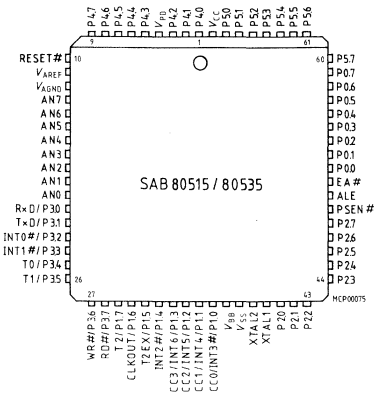
Preliminary

Extended Temperature Ranges:

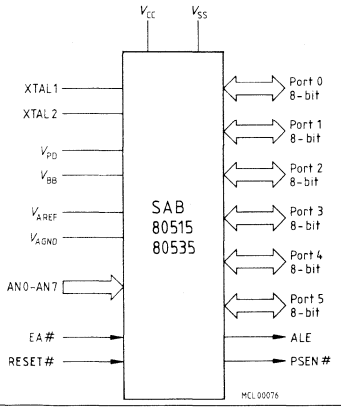
	T40/85	**– 40 to + 85 °C 12 MHz operation**
	T40/110	**– 40 to + 110 °C 12 MHz operation**
SAB 80515-N- T40/85	**Microcontroller with factory mask-programmable ROM**	
SAB 80515-N- T40/110		
SAB 80535-N- T40/85	**Microcontroller for external ROM**	
SAB 80535-N- T40/110		

- Version of the SAB 80515/80535 for two extended temperature ranges
- 8K × 8 ROM (SAB 80515 only)
- 256 × 8 RAM
- Six 8-bit I/O ports, one 8-bit input port for analog signals
- Three 16-bit timer/counters
- Highly flexible reload, capture, compare capabilities
- Full-duplex serial channel
- Twelve interrupt vectors, four priority levels
- 8-bit A/D converter with eight multiplexed inputs and programmable internal reference voltages
- 16-bit watchdog timer
- V_{PD} provides standby current for 40 bytes of RAM
- Boolean processor
- 256 bit-addressable locations
- Most instructions execute in 1 µs
- 4 µs multiply and divide
- External memory expandable up to 128 Kbyte
- Backwardly compatible with SAB 8051
- 68-pin plastic leaded chip carrier package (PL-CC-68)

Pin Configuration



Logic Symbol



The SAB 80515/80535 Ext. Temp. is a powerful member of the Siemens SAB 8051 family of 8-bit microcontrollers. The The SAB 80515/80535 Ext. Temp. is available for the industrial temperature range (– 40 to + 85 °C) and the automotive temperature range (– 40 to + 110 °C). It is fully compatible with the standard SAB 80515/80535 with respect to architecture, instruction set and software portability. The SAB 80515/80535 Ext. Temp. is a stand-alone, high-performance single-chip microcontroller designed in + 5 V N-channel, silicon-gate Siemens MYMOS technology. While maintaining all the SAB 8051 operating characteristics, the SAB 80515/80535 Ext Temp. incorporates several enhancements which significantly increase design flexibility and overall system performance.
The SAB 80535 is identical with the SAB 80515 except that it lacks the on-chip program memory. The SAB 80515/80535 Ext. Temp. is supplied in a 68-pin plastic leaded chip carrier package PL-CC-68.

Ordering Information

Type	Ordering code	Package	Description
			8-bit single-chip microcontroller
SAB 80515-N-T40/85	Q67120-C210	PL-CC-68	with mask-programmable ROM
SAB 80535-N-T40/85	Q67120-C240	PL-CC-68	for external memory
SAB 80515-N-T40/110	Q67120-C316	PL-CC-68	with mask-programmable ROM
SAB 80535-N-T40/110	Q67120-C313	PL-CC-68	for external memory

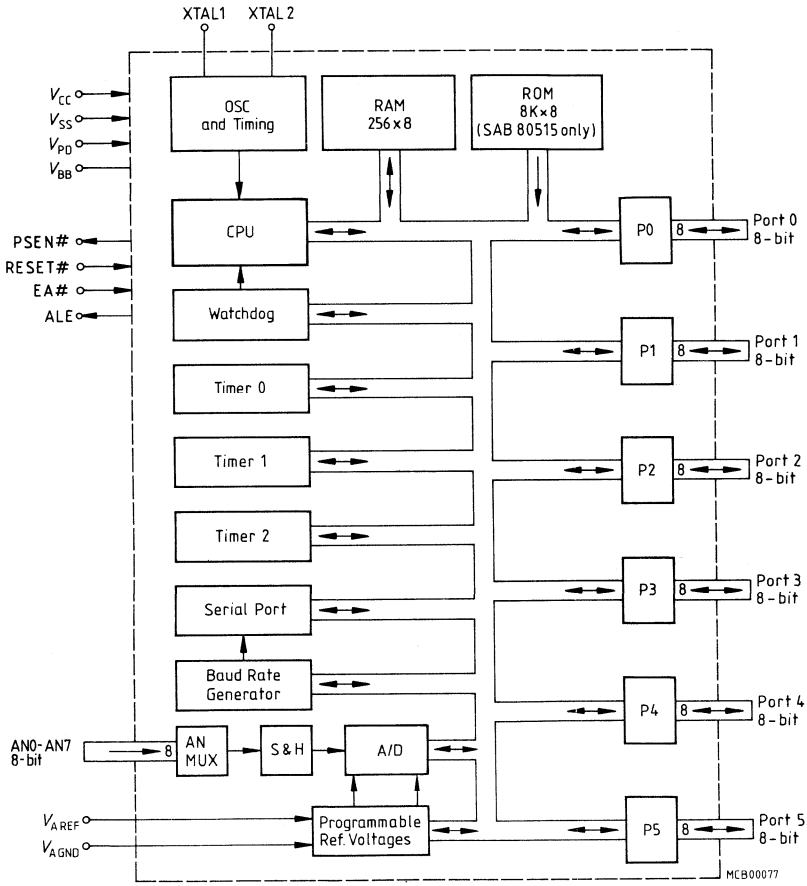
Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	I/O	Port 4 is an 8-bit quasi-bidirectional I/O port. Port 4 can sink/source 4 LS-TTL loads.
V_{PD}	4		Power down supply. If V_{PD} is held within its specs while V_{CC} drops below specs, V_{PD} will provide standby power to 40 byte of the internal RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
$\overline{\text{RESET}}$	10	I	A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80515. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	11		Reference voltage for the A/D converter
V_{AGND}	12		Reference ground for the A/D converter
AN7-AN0	13-20	I	Multiplexed analog inputs
P3.0-P3.7	21-28	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source 4 LS-TTL loads. The secondary functions are assigned to the pins of port 3, as follows: – R_xD (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – T_xD (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – $\overline{\text{INT0}}$ (P3.2): interrupt 0 input / timer 0 gate control input – $\overline{\text{INT1}}$ (P3.3): interrupt 1 input / timer 1 gate control input – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – $\overline{\text{WR}}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory – $\overline{\text{RD}}$ (P3.7): the read control signal enables the external data memory to port 0
P1.7-P1.0	29-36	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. It also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch must be programmed to a one (1) for that function to operate (except when used for the compare functions). Port 1 can sink/source 4 LS-TTL loads. The secondary functions are assigned to the port 1 pins, as follows: – $\overline{\text{INT3}}$/CC0 (P1.0): interrupt 3 input/compare 0 output/ capture 0 input – INT4/CC1 (P1.1): interrupt 4 input/compare 1 output/ capture 1 input – INT5/CC2 (P1.2): interrupt 5 input/compare 2 output/ capture 2 input – INT6/CC3 (P1.3): interrupt 6 input/compare 3 output/ capture 3 input

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P1.7-P1.0 (cont'd)			– $\overline{INT2}$ (P1.4): interrupt 2 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input
V_{BB}	37		Substrate pin. Must be connected to V_{SS} through a capacitor (47 to 100 nF) for proper operation of the A/D converter.
XTAL2	39		XTAL2 is the output from the oscillator's amplifier.Input to the internal timing circuitry. A crystal, ceramic resonator, or external source can be used.
XTAL1	40		XTAL1 is the input to the oscillator's high gain amplifier. Required when a crystal or ceramic resonator is used. Connect to V_{SS} when external source is used on XTAL2.
P2.0-P2.7	41-48	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source 4 LS-TTL loads.
$\overline{PSEN}$	49	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during internal program execution.
ALE	50	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{EA}$	51	I	When held at a TTL high level, the SAB 80515 executes instructions from the internal ROM when the PC is less than 8192. When held at a TTL low level, the SAB 80515 fetches all instructions from external program memory. For the SAB 80535 this pin must be tied low.
P0.0-P0.7	52-59	I/O	Port 0 is an 8-bit open-drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source 8 LS-TTL loads.
P5.7-P5.0	60-67	I/O	Port 5 is an 8-bit quasi-bidirectional I/O port. Port 5 can sink/source 4 LS-TTL loads.
V_{CC}	68		POWER SUPPLY (+ 5 V power supply during normal operation and program verification)
V_{SS}	38		GROUND (0 V)

Figure 1
Block Diagram



Functional Description

The members of the SAB 80515 family of microcontrollers are:

- SAB 80515: Microcontroller, designed in Siemens MYMOS technology, with 8 Kbyte factory mask-programmable ROM
- SAB 80535: ROM-less version of the SAB 80515
- SAB 80C515: Microcontroller, designed in Siemens ACMOS technology, with 8 Kbyte factory mask-programmable ROM
- SAB 80C535: ROM-less version of the SAB 80C515
- SAB 80515K: Special ROM-less version of the SAB 80515 with an additional interface for program memory accesses. An external ROM that is accessed via this interface substitutes the SAB 80515's internal ROM.

The SAB 80535 is identical to the SAB 80515, except that it lacks the on-chip ROM. In this data sheet the term "SAB 80515" is used to refer to both the SAB 80515 and SAB 80535, unless otherwise noted.

Principles of Architecture

The architecture of the SAB 80515 is based on the SAB 8051 microcontroller family. The following features of the SAB 80515 are fully compatible with the SAB 8051 features:
- Instruction set
- External memory expansion interface (port 0 and port 2)
- Full-duplex serial port
- Timer/counter 0 and 1
- Alternate functions on port 3
- The lower 128 bytes of internal RAM and the lower 4 Kbytes of internal ROM

The SAB 80515 additionally contains 128 bytes of internal RAM and 4 Kbytes of internal ROM, which results in a total of 256 bytes of RAM and 8 Kbytes of ROM on chip. The SAB 80515 has a new 16-bit timer/counter with a 2:1 prescaler, reload mode, compare and capture capability. It also contains a 16-bit watchdog timer, an 8-bit A/D converter with programmable reference voltages, two additional quasi-bidirectional 8-bit ports, one 8-bit input port for analog signals, and a programmable clock output ($f_{OSC}/12$). Furthermore, the SAB 80515 has a powerful interrupt structure with 12 vectors and 4 programmable priority levels.
Figure 1 shows a block diagram of the SAB 80515.

CPU

The SAB 80515 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1.0 µs.

Memory Organization

The SAB 80515 manipulates operands in the four memory address spaces described below: (Figure 2 illustrates the memory address spaces of the SAB 80515).

Program memory

The SAB 80515 has 8 Kbyte of on-chip ROM, while the SAB 80535 has no internal ROM. The program memory can be externally expanded up to 64 Kbytes. If the $\overline{EA}$ pin is held high, the SAB 80515 executes out of internal ROM unless the address exceeds 1FFFH. Locations 2000H through 0FFFFH are then fetched from the external program memory. If the $\overline{EA}$ pin is held low, the SAB 80515 fetches all instructions from the external program memory. Since the SAB 80535 has no internal ROM, pin $\overline{EA}$ must be tied low when using this component.

Data Memory

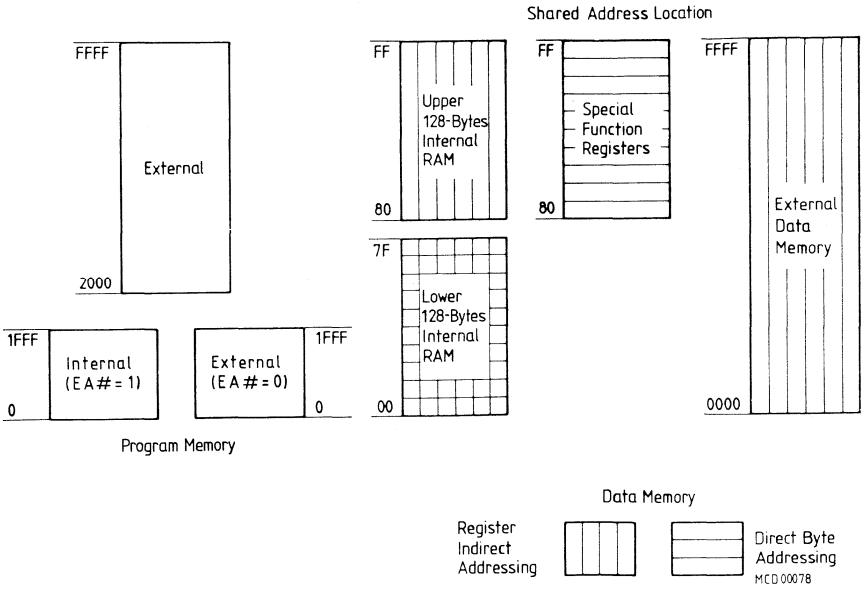
The data memory address space consists of an internal and an external memory space. The internal data memory is divided into three physically separate and distinct blocks: the lower 128 bytes of RAM, the upper 128 bytes of RAM, and the 128-byte special function register (SFR) area. While the upper 128 bytes of data memory and the SFR area share the same address locations, they are accessed through different addressing modes. The lower 128 bytes of data memory can be accessed through direct or register indirect addressing; the upper 128 bytes of RAM can be accessed through register indirect addressing; the special function registers are accessible through direct addressing.
Four 8-register banks, each bank consisting of eight 8-bit multi-purpose registers, occupy locations 0 through 1FH in the lower RAM area. The next 16 bytes, locations 20H through 2FH, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal data memory address space, and the stack depth can be expanded up to 256 bytes.
The external data memory can be expanded up to 64 Kbytes and can be accessed by instructions that use a 16-bit or an 8-bit address.

All registers, except the program counter and the four 8-register banks, reside in the special function register area. The 41 special function registers (SFR's) include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripheral functions. There are also 128 directly addressable bits within the SFR area. The special function registers are listed in the following table:

Symbol	Name	Address
* P0	Port 0	80H
SP	Stack pointer	81H
DPL	Data pointer, low byte	82H
DPH	Data pointer, high byte	83H
PCON	Power control register	87H
* TCON	Timer control register	88H
TMOD	Timer mode register	89H
TL0	Timer 0, low byte	8AH
TL1	Timer 1, low byte	8BH
TH0	Timer 0, high byte	8CH
TH1	Timer 1, high byte	8DH
* P1	Port 1	90H
* SCON	Serial port control register	98H
SBUF	Serial port buffer register	99H
* P2	Port 2	0A0H
* IEN0	Interrupt enable register 0	0A8H
IP0	Interrupt priority register 0	0A9H
* P3	Port 3	0B0H
* IEN1	Interrupt enable register 1	0B8H
IP1	Interrupt priority register 1	0B9H
* IRCON	Interrupt request control register	0C0H
CCEN	Compare/capture enable register	0C1H
CCL1	Compare/capture register 1, low byte	0C2H
CCH1	Compare/capture register 1, high byte	0C3H
CCL2	Compare/capture register 2, low byte	0C4H
CCH2	Compare/capture register 2, high byte	0C5H
CCL3	Compare/capture register 3, low byte	0C6H
CCH3	Compare/capture register 3, high byte	0C7H
* T2CON	Timer 2 control register	0C8H
CRCL	Compare/reload/capture register, low byte	0CAH
CRCH	Compare/reload/capture register, high byte	0CBH
TL2	Timer 2, low byte	0CCH
TH2	Timer 2, high byte	0CDH
* PSW	Program status word register	0D0H
* ADCON	A/D-converter control register	0D8H
ADDAT	A/D-converter data register	0D9H
DAPR	D/A-converter program register	0DAH
* ACC	Accumulator	0E0H
* P4	Port 4	0E8H
* B	B register	0F0H
* P5	Port 5	0F8H

The SFR's marked with an asterisk (*) are both bit and byte-addressable.

Figure 2
Memory Address Spaces



I/O Ports

The SAB 80515 has six 8-bit I/O ports and one 8-bit input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pull-up resistors. That means, when configured as inputs, ports 1 to 5 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.
Ports 1 and 3 are provided for several alternate functions, as listed below:

Port	Symbol	Function
P1.0	$\overline{\text{INT3}}$/CC0	External interrupt 3 input, compare 0 output, capture 0 input
P1.1	INT4/CC1	External interrupt 4 input, compare 1 output, capture 1 input
P1.2	INT5/CC2	External interrupt 5 input, compare 2 output, capture 2 input
P1.3	$\overline{\text{INT6}}$/CC3	External interrupt 6 input, compare 3 output, capture 3 input
P1.4	$\overline{\text{INT2}}$	External interrupt 2 input
P1.5	T2EX	Timer 2 external reload trigger input
P1.6	CLKOUT	System clock output
P1.7	T2	Timer 2 external counter input
P3.0	RXD	Serial port's receiver data input (asynchronous) or data input/output (synchronous)
P3.1	TXD	Serial port's transmitter data output (asynchronous) or clock output (synchronous)
P3.2	$\overline{\text{INT0}}$	External interrupt 0 input, timer 0 gate control
P3.3	$\overline{\text{INT1}}$	External interrupt 1 input, timer 1 gate control
P3.4	T0	Timer 0 external counter input
P3.5	T1	Timer 1 external counter input
P3.6	$\overline{\text{WR}}$	External data memory write strobe
P3.7	$\overline{\text{RD}}$	External data memory read strobe

The input port AN0-AN7 is used for analog input signals to the A/D converter.

Timer/Counters

The SAB 80515 contains three 16-bit timer/counters which are useful in many applications for timing and counting. The input clock for each timer/counter is 1/12 of the oscillator frequency in the timer operation or can be taken from an external clock source for the counter operation (maximum count rate is 1/24 of the oscillator frequency).

Timer/counter 0 and 1

These timer/counters can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto-reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; timer/counter 1 in this mode holds its count.

External inputs $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

Timer/counter 2

Timer/counter 2 of the SAB 80515 is a 16-bit timer/counter with several additional features. It offers a 2:1 prescaler, a selectable gate function, and compare, capture and reload functions. Corresponding to the 16-bit timer register there are four 16-bit capture/compare registers, one of them can be used to perform a 16-bit reload on a timer overflow or external event. Each of these registers corresponds to a pin of port 1 for capture input/compare output.

Figure 3 shows a block diagram of the timer/counter 2.

– Reload

A 16-bit reload can be performed with the 16-bit CRC register, which is a concatenation of the 8-bit registers CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer 2 overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

– Capture

This feature permits saving the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value in timer 2 registers into a dedicated capture register:

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

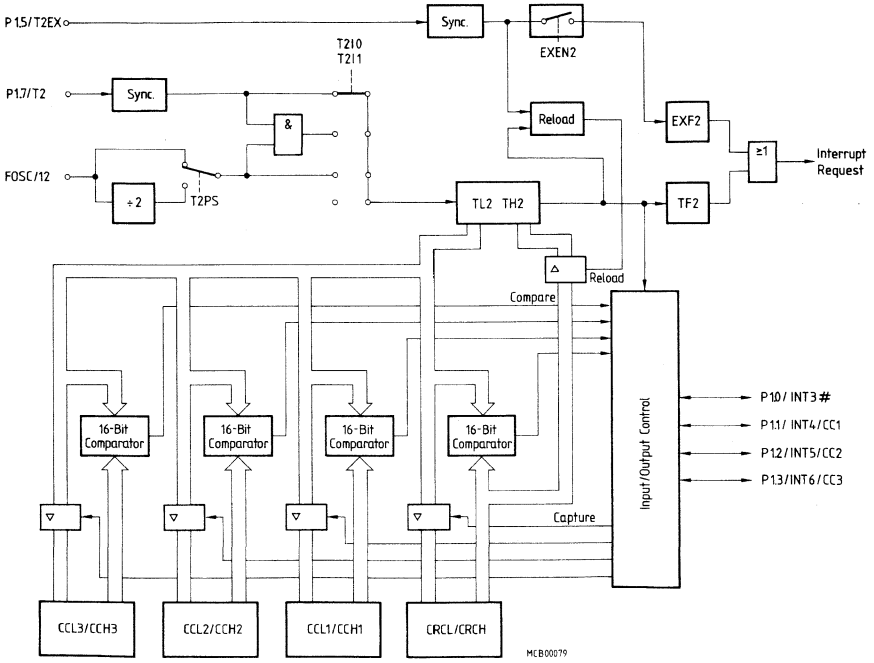
– Compare

In the compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 registers. If the count value in the timer 2 registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to a low level when timer 2 overflows.

Mode 1: The transition of the output signal can be determined by software. A timer 2 overflow causes no output change.

Figure 3
Block Diagram of Timer/Counter 2



Serial Port

The serial port of the SAB 80515 enables full duplex communication between microcontrollers or between microcontroller and peripheral devices. The serial port can operate in 4 modes:

Mode 0: Shift register mode. Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 10 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). The baud rate is variable.

Mode 2: 11 bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Mode 3 is identical to mode 2 except for the baud rate. The baud rate in mode 3 is variable.

The variable baud rates in modes 1 and 3 can be generated by timer 1 or an internal baud rate generator.

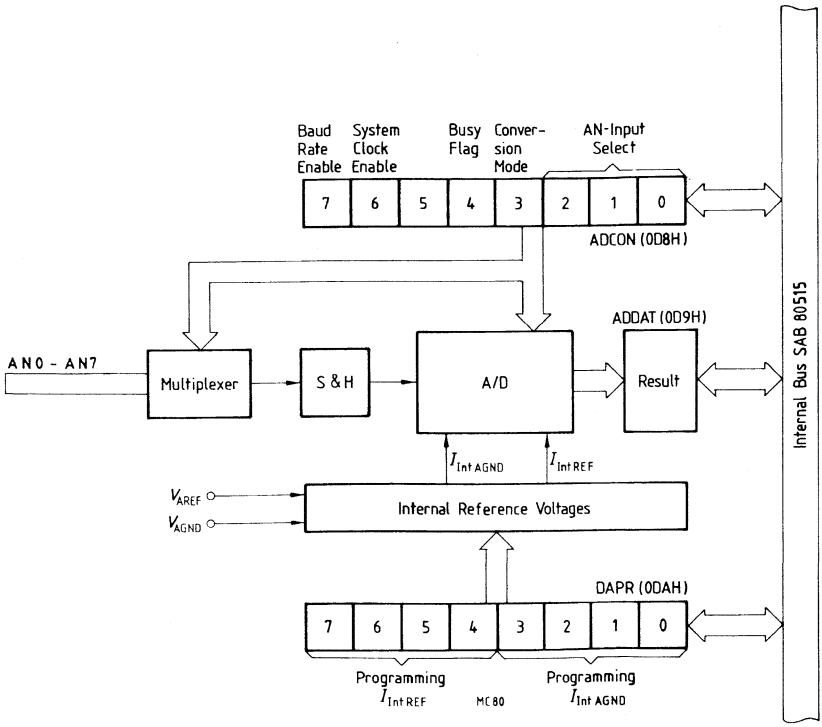
A/D Converter

The 8-bit A/D converter of the SAB 80515 has eight multiplexed analog inputs (Port 6) and uses the successive approximation method.
It takes 5 machine cycles to sample an analog signal (during this sample time the input signal should be held constant); the total conversion time (including sample time) is 15 machine cycles (15 µs at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous; at the end of a conversion an interrupt can be generated.

A unique feature is the capability of internal reference voltage programming. The internal reference voltages $V_{IntAREF}$ and $V_{IntAGND}$ for the A/D converter both are programmable to one of 16 steps with respect to the external reference voltages. This feature permits a conversion with a smaller internal reference voltage range to gain a higher resolution. In addition, the internal reference voltages can easily be adapted by software to the desired analog input voltage range.

Figure 4 shows a block diagram of the A/D converter.

Figure 4
Block Diagram of the A/D Converter



Interrupt Structure

The SAB 80515 has 12 interrupt vectors with the following vector addresses and request flags:

Table 2
Interrupt Sources and Vectors

Source (Request Flags)	Vector	Vector address
IE0	External interrupt 0	0003H
TF0	Timer 0 interrupt	000BH
IE1	External interrupt 1	0013H
TF1	Timer 1 interrupt	001BH
RI + TI	Serial port interrupt	0023H
TF2 + EXF2	Timer 2 interrupt	002BH
IADC	A/D converter interrupt	0043H
IEX2	External interrupt 2	004BH
IEX3	External interrupt 3	0053H
IEX4	External interrupt 4	005BH
IEX5	External interrupt 5	0063H
IEX6	External interrupt 6	006BH

Each interrupt vector can be individually enabled/disabled. The minimum response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles.

Figure 5 shows the interrupt request sources.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 3 to 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs. Each pair can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1. Figure 6 shows the priority level structure.

Figure 5
Interrupt Request Sources

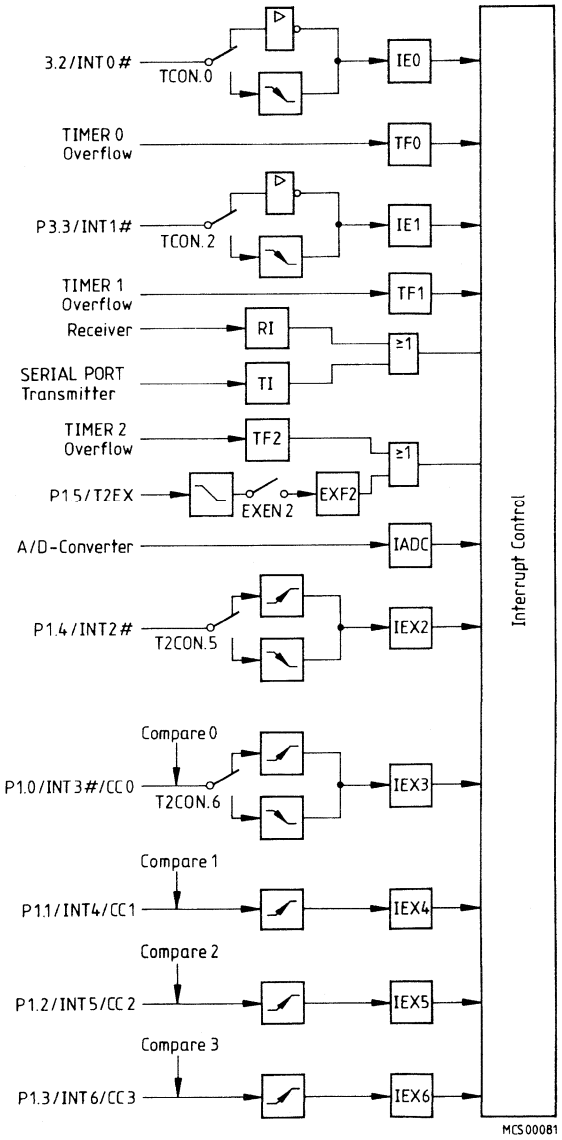
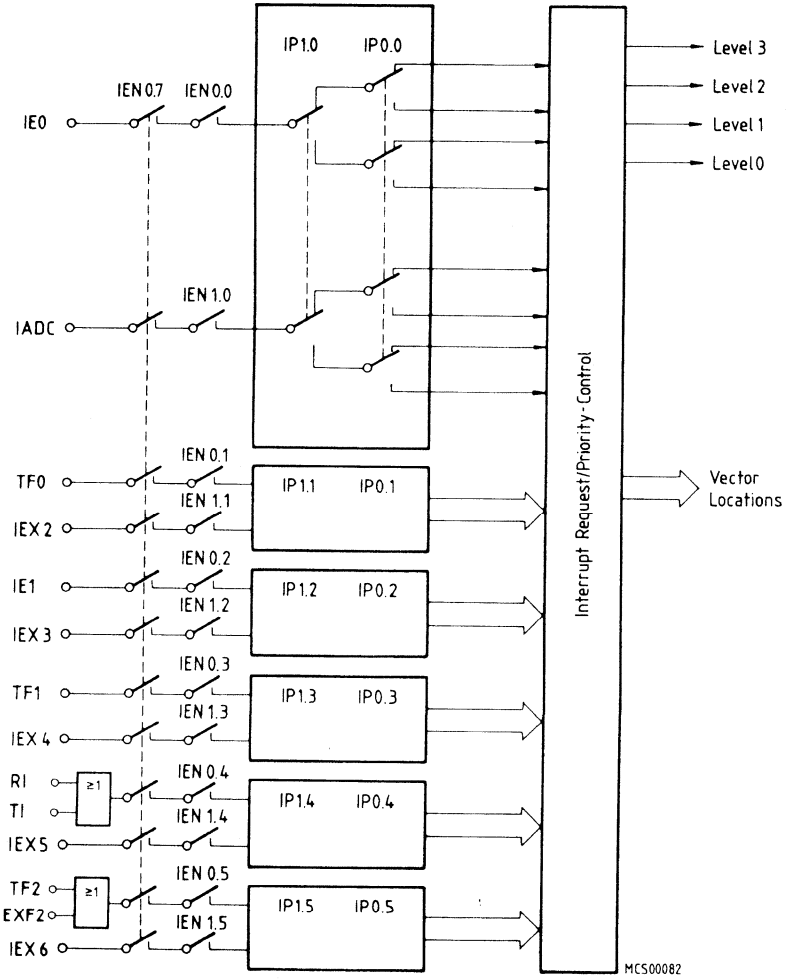


Figure 6
Priority Level Structure



Watchdog Timer

This feature is provided as a means of graceful recovery from a software upset. After an external reset, the watchdog timer is cleared and stopped. It can be started and cleared by software, but it cannot be stopped. If the software fails to clear the watchdog timer at least every 65532 machine cycles (about 65 ms if a 12 MHz oscillator frequency is used), an internal hardware reset will be initiated.

The reset cause (external reset or reset caused by the watchdog) can be examined by software. To clear the watchdog, two bits in two different special function registers must be set by two consecutive instructions (bits IEN0.6 and IEN1.6). This is done to prevent the watchdog from being cleared by unexpected opcodes.

Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations				
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct*)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct, A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A, ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer				
MOV	direct,@R	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A + DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0 – R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is + 127/– 128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr,code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr,code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,*#data*
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr,code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,*#data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr,#data*
44	2	ORL	A,*#data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr,#data*
54	2	ANL	A,*#data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr,#data*
64	2	XRL	A,*#data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr*,*data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*,R2
8B	2	MOV	*data addr*,R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data*,*code addr*
B5	3	CJNE	A,*data addr*,*code addr*
B6	3	CJNE	@R0,#*data*,*code addr*
B7	3	CJNE	@R1,#*data*,*code addr*
B8	3	CJNE	R0,#*data*,*code addr*
B9	3	CJNE	R1,#*data*,*code addr*
BA	3	CJNE	R2,#*data*,*code addr*
BB	3	CJNE	R3,#*data*,*code addr*
BC	3	CJNE	R4,#*data*,*code addr*
BD	3	CJNE	R5,#*data*,*code addr*
BE	3	CJNE	R6,#*data*,*code addr*
BF	3	CJNE	R7,#*data*,*code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr**)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr*,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	– 40 to + 85 °C for SAB 80515/80535-T40/85 – 40 to + 110 °C for SAB 80515/80535-T40/110
Storage temperature	– 65 to + 150 °C
Voltage on any pin with respect to ground (V_{SS})	– 0.5 to + 7 V
Power dissipation	2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V; T_A = – 40 to + 85 °C for SAB 80515/80535-T40/85
T_A = – 40 to + 110 °C for SAB 80515/80535-T40/110

Symbol	Parameter	Limit Values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	– 0.5	0.8	V	–
V_{IH}	Input high voltage (except RESET and XTAL2)	2.0	V_{CC} + 0.5	V	–
V_{IH1}	Input high voltage to XTAL2	2.5	V_{CC} + 0.5	V	XTAL1 to V_{SS}
V_{IH2}	Input high voltage to $\overline{\text{RESET}}$	3.0	–	V	–
V_{PD}	Power down voltage	3	5.5	V	V_{CC} = 0 V
V_{OL}	Output low voltage, ports 1, 2, 3, 4, 5	–	0.45	V	I_{OL} = 1.6 mA [1]
V_{OL1}	Output low voltage, port 0, ALE, $\overline{\text{PSEN}}$	–	0.45	V	I_{OL} = 3.2 mA [1]
V_{OH}	Output high voltage, ports 1, 2, 3, 4, 5	2.4	–	V	I_{OH} = – 80 µA
V_{OH1}	Output high voltage, port 0, ALE, $\overline{\text{PSEN}}$	2.4	–	V	I_{OH} = – 400 µA
I_{IL}	Logic 0 input current, ports 1, 2, 3, 4, 5	–	– 800	µA	V_{IL} = 0.45 V
I_{IL2}	Logic 0 input current, XTAL2	–	– 2.5	mA	XTAL1 = V_{SS} V_{IL} = 0.45 V
I_{IL3}	Input low current to $\overline{\text{RESET}}$ for reset	–	– 500	µA	V_{IL} = 0.45 V
I_{LI}	Input leakage current to port 0, $\overline{\text{EA}}$	–	± 10	µA	0 V < V_{IN} < V_{CC}
I_{CC}	Power supply current SAB 80515/80535-T40/85 SAB 80515/80535-T40/110	 – –	 230 230	 mA	all outputs disconnected
I_{PD}	Power down current	–	3	mA	V_{CC} = 0 V
C_{IO}	Capacitance of I/O buffer	–	10	pF	f_C = 1 MHz

[1]) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1, 3, 4, 5. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-0 transcitions during bus operation.

A/D Converter Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V; V_{AREF} = V_{CC} ± 5 %; V_{AGND} = V_{SS} ± 0.2 V; $V_{IntAREF} - V_{IntAGND} \geq 1$ V;
T_A = – 40 to + 85 °C for SAB 80515/80535-T40/85
T_A = – 40 to + 110 °C for SAB 80515/80535-T40/110

Symbol	Parameter	Limit Values			Unit	Test condition
		min.	typ.	max.		
V_{AINPUT}	Analog input voltage	V_{AGND}- 0.2	–	V_{AREF}+ 0.2	V	–
C_I	Analog input capacitance	–	25	–	pF	2)
t_L	Load time	–	–	2 t_{CY}	–	–
t_S	Sample time (incl. load time)	–	–	5 t_{CY}	–	–
t_C	Conversion time (including sample time)	–	–	15 t_{CY}	–	–
DNLE	Differential non-linearity	–	± 1/2	± 1	LSB	$V_{IntAREF}$ = V_{AREF} = V_{CC} $V_{IntAGND}$ = V_{AGND} = V_{SS}
INLE	Integral non-linearity	–	± 1/2	± 1	LSB	
	Offset error	–	± 1/2	± 1	LSB	
	Gain error	–	± 1/2	± 1	LSB	
TUE	Total unadjusted error	–	–	± 2	LSB	3)
I_{REF}	V_{AREF} supply current	–	–	5	mA	3)
$V_{IntREF\ ERR}$	Internal reference error	–	± 5	± 15	mV	3)

2) The output impedance of the analog source must be low enough to assure full loading of the sample capacitance (C_I) during load time (t_L). After charging of the internal capacitance (C_I) during load time (t_L) the analog input must be held constant for the rest of the sample time (t_S).

3) The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

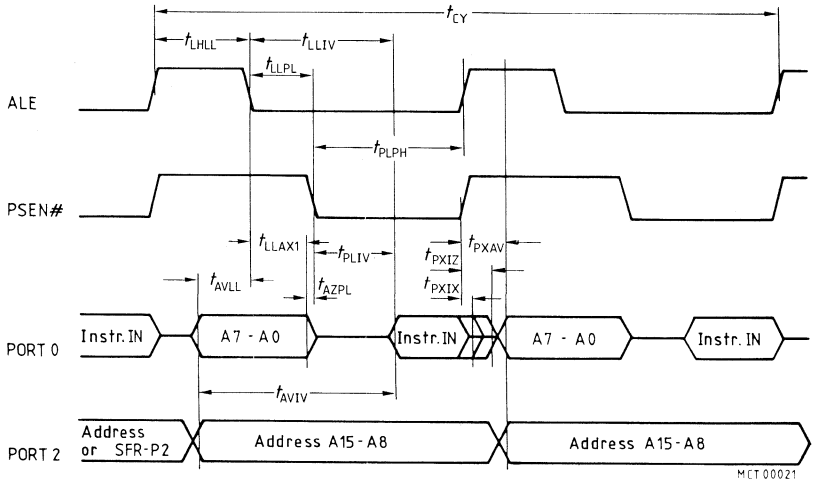
AC Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
T_A = – 40 to + 85 °C for SAB 80515/80535-T40/85
T_A = – 40 to + 110 °C for SAB 80515/80535-T40/110
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

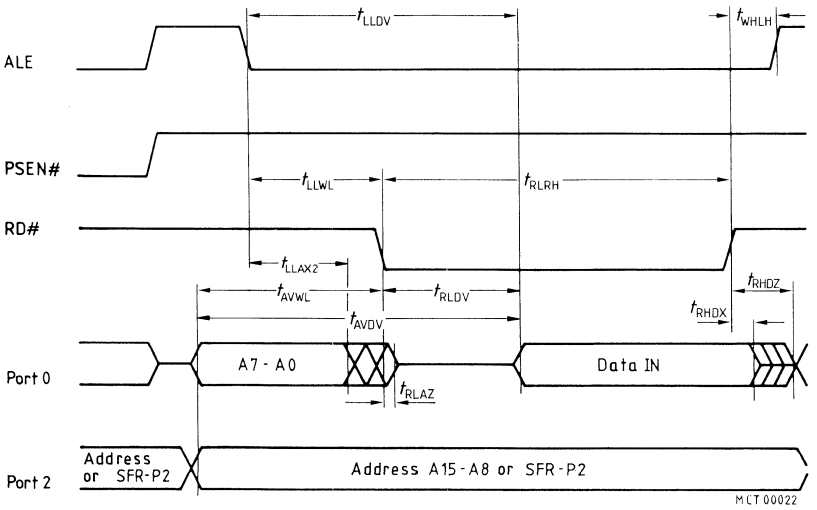
Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
t_{ICY}	Cycle time	1000	–	12 t_{CLCL}	–	ns
t_{LHLL}	ALE pulse width	127	–	2 t_{CLCL} – 40	–	ns
t_{AVLL}	Address setup to ALE	53	–	t_{CLCL} – 30	–	ns
t_{LLAX1}	Address hold after ALE	48	–	t_{CLCL} – 35	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	4 t_{CLCL} – 100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	58	–	t_{CLCL} – 25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	3 t_{CLCL} – 35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	150	–	3 t_{CLCL} – 100	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ} *)	Input instruction float after $\overline{PSEN}$	–	63	–	t_{CLCL} – 20	ns
t_{PXAV} *)	Address valid after $\overline{PSEN}$	75	–	t_{CLCL} – 8	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	5 t_{CLCL} – 115	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns
External Data Memory Characteristics						
t_{RLRH}	$\overline{RD}$ pulse width	400	–	6 t_{CLCL} – 100	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	6 t_{CLCL} – 100	–	ns
t_{LLAX2}	Address hold after ALE	132	–	2 t_{CLCL} – 35	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	252	–	5 t_{CLCL} – 165	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	2 t_{CLCL} – 70	ns
t_{LLDV}	ALE to valid data in	–	517	–	8 t_{CLCL} – 150	ns
t_{AVDV}	Address to valid data in	–	585	–	9 t_{CLCL} – 165	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	4 t_{CLCL} – 130	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	t_{CLCL} – 40	t_{CLCL} + 40	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	33	–	t_{CLCL} – 50	–	ns
t_{QVWX}	Data setup before $\overline{WR}$	433	–	7 t_{CLCL} – 150	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	t_{CLCL} – 50	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

*) Interfacing the SAB 80515 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

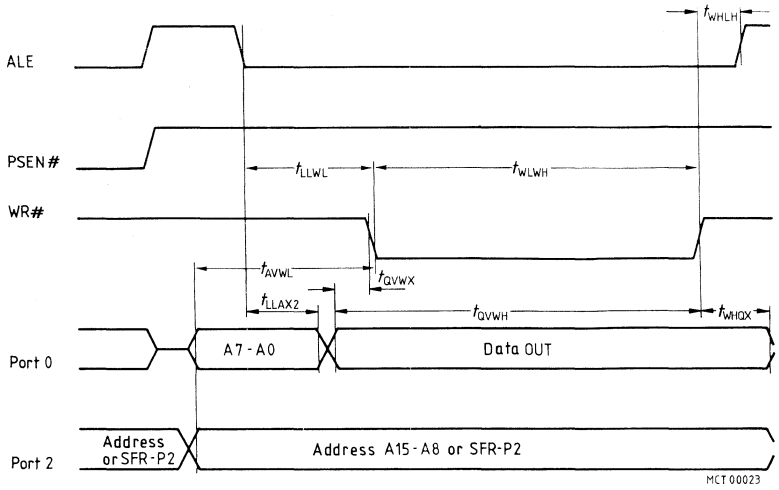
Program Memory Read Cycle



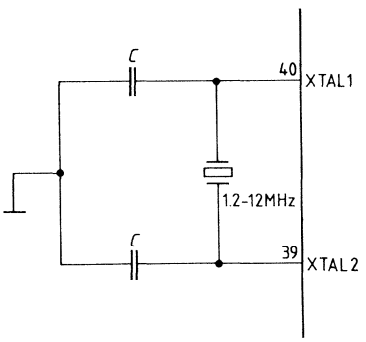
Data Memory Read Cycle



Data Memory Write Cycle

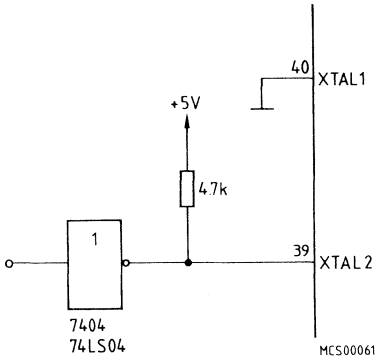


Recommended Oscillator Circuits



$C = 30pF \pm 10pF$

Crystal Oscillator Mode

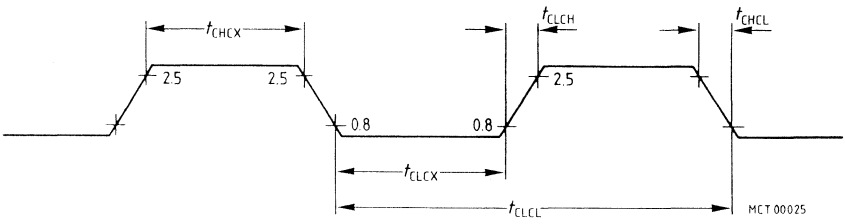


Driving from External Source

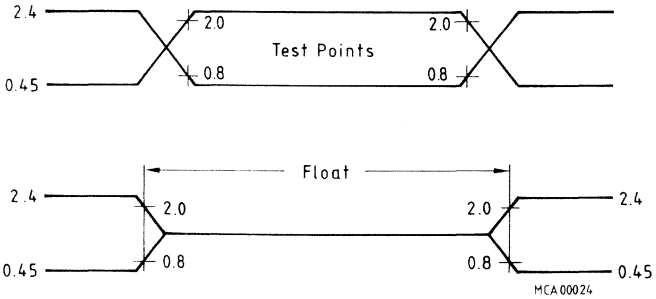
External Clock Drive XTAL2

Symbol	Parameter	Limit Values		Unit
		Variable clock Frequ. = 1.2 MHz to 16 MHz		
		min.	max.	
t_{CLCL}	Oscillator period	83.3	833.3	ns
t_{CHCX}	High time	20	$t_{CLCL} - t_{CLCX}$	ns
t_{CLCX}	Low time	20	$t_{CLCL} - t_{CHCX}$	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

External Clock Cycle



A.C. Testing Input, Output, Float Waveforms

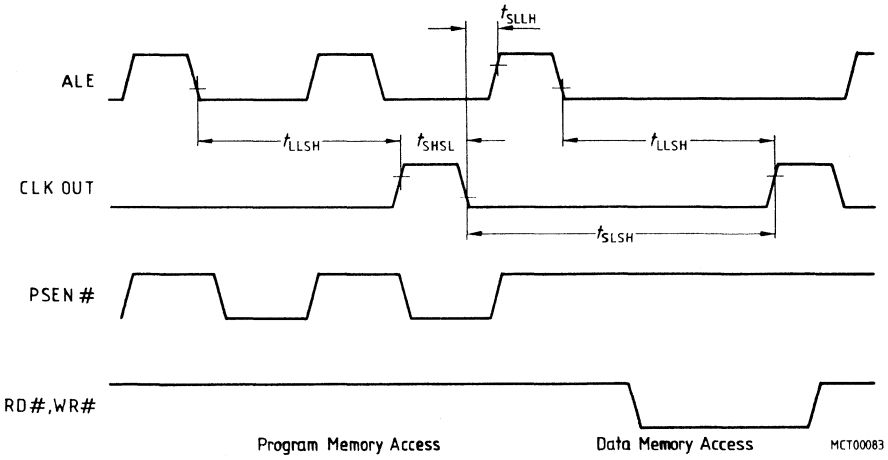


A.C. testing inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point where a P0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels.

System Clock Timing

Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{LLSH}	ALE to CLKOUT	543	–	$7t_{CLCL} - 40$	–	ns
t_{SHSL}	CLKOUT high time	127	–	$2t_{CLCL} - 40$	–	ns
t_{SLSH}	CLKOUT low time	793	–	$10t_{CLCL} - 40$	–	ns
t_{SLLH}	CLKOUT low to ALE high	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns

System Clock Timing

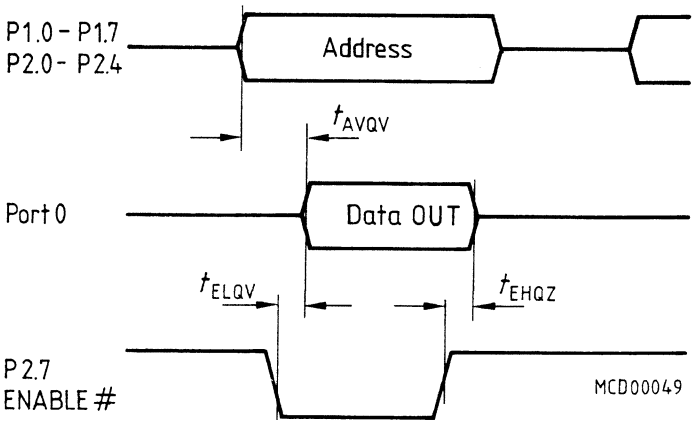


ROM Verification Characteristics

T_A = 25 °C ± °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	$48t_{CLCL}$	ns
t_{ELQV}	ENABLE to valid data	–	$48t_{CLCL}$	ns
t_{EHQZ}	Data float after ENABLE	0	$48t_{CLCL}$	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification



Address: P1.0-P1.7 = A0-A7
P2.0-P2.4 = A8-A12

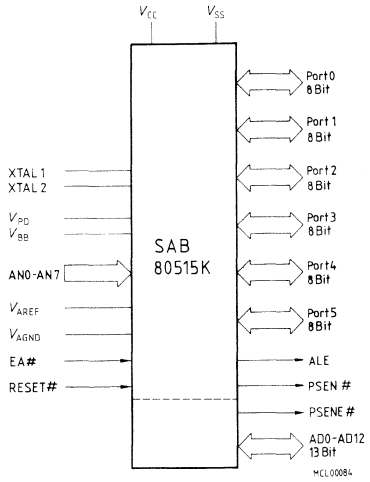
Data: Port 0 = D0-D7

Inputs: P2.5-P2.6, $\overline{PSEN}$ = V_{SS}
ALE, $\overline{EA}$ = V_{IH}
RESET = V_{IL}

8-Bit Single Chip Microcontroller ROM-less Version SAB 80515K

- Additional bus interface for external memory
- 256 × 8 RAM
- Six 8-bit ports
- Three 16-bit timer/event counters
- Highly flexible reload, capture, compare capabilities
- Full-duplex serial channel
- Twelve interrupt sources, four priority levels
- 8-bit A/D converter with 8 multiplexed analog inputs and programmable internal reference voltages
- 16-bit watchdog time
- V_{PD} provides standby current for 40 bytes of RAM
- Boolean processor
- 256 bit-addressable locations
- Most instructions execute in 1 µs
- 4 µs multiply and divide
- External memory expandable to 128 Kbyte
- Pin grid array package, 88 pins (C-PGA-88)

Logic Symbol



The SAB 80515K is a special ROM-less version of the 8-bit microcontroller SAB 80515. The SAB 80515K contains an additional bus interface to connect an external program memory in place of the SAB 80515's on-chip ROM. Thereby, the SAB 80515K maintains the full I/O capability of the single-chip SAB 80515 while it permits connection of an external program memory. All other features of the SAB 80515K are identical with those of the SAB 80515. The SAB 80515K is fabricated in + 5 V advanced N-channel, silicon gate Siemens MYMOS technology, and supplied as pin grid array with 88 pins (C-PGA-88).

8-Bit CMOS Microcontroller — SAB 80C515/80C535

Advance Information

SAB 80C515/80C515-16	CMOS microcontroller with factory mask-programmable ROM
SAB 80C535/80C535-16	CMOS microcontroller for external ROM
SAB 80C515-T40/110, SAB 80C535-T40/110	Extended temperature range: – 40 to + 110°C (for 12 MHz)
SAB 80C515-T40/85, SAB 80C535-T40/85	Extended temperature range: – 40 to + 85°C (for 12 MHz)
SAB 80C515-16-T40/85, SAB 80C535-16-T40/85	Extended temperature range: – 40 to + 85°C (for 16 MHz)

- 8 K × 8 ROM (SAB 80C515 only)
- 256 × 8 RAM
- Six 8-bit I/O ports, one input port for digital or analog input
- Three 16-bit timer/counters
- Highly flexible reload, capture, compare capabilities
- Full-duplex serial channel
- Twelve interrupt vectors, four priority levels
- 8-bit A/D converter with 8 multiplexed inputs and programmable internal reference voltages
- 16-bit watchdog timer
- Boolean processor
- 256-bit-addressable locations
- Most instructions execute in 1 µs (750 ns)
- 4 µs (3 µs) multiply and divide
- External memory expandable up to 128 Kbytes
- Backwardly compatible with SAB 8051
- Functionally compatible with SAB 80515
- Idle and power-down mode
- 68-pin plastic leaded chip carrier package (PL-CC-68)

Ordering Information

Type	Ordering code	Package	Description
			8-bit CMOS microcontroller
SAB 80C515-N	Q 67120-C297	PL-CC-68	with mask-programmable ROM, 12 MHz
SAB 80C535-N	Q 67120-C508	PL-CC-68	for external memory, 12 MHz
SAB 80C515-N-T40/85	Q 67120-C388	PL-CC-68	with mask-programmable ROM, 12 MHz ext. temperature – 40 to + 85 °C
SAB 80C535-N-T40/85	Q 67120-C510	PL-CC-68	for external memory, 12 MHz ext. temperature – 40 to + 85 °C
SAB 80C515-N-T40/110	Q 67120-C391	PL-CC-68	with mask-programmable ROM, 12 MHz ext. temperature – 40 to + 110 °C
SAB 80C535-N-T40/110	Q 67120-C538	PL-CC-68	for external memory, 12 MHz ext. temperature – 40 to + 110 °C
SAB 80C515-16-N	Q 67120-C492	PL-CC-68	with mask-programmable ROM, 16 MHz
SAB 80C535-16-N	Q 67120-C509	PL-CC-68	for external memory, 16 MHz
SAB 80C515-16-N-T40/85	Q 67120-C561	PL-CC-68	with mask-programmable ROM, 16 MHz ext. temperature – 40 to + 85 °C
SAB 80C535-16-N-T40/85	Q 67120-C562	PL-CC-68	for external memory, 16 MHz ext. temperature – 40 to + 85 °C

The SAB 80C515/80C535 is a new, powerful member of the Siemens SAB 8051 family of 8-bit microcontrollers. It is designed in Siemens ACMOS technology and is functionally compatible with the SAB 80515/80535 devices designed in MYMOS technology.

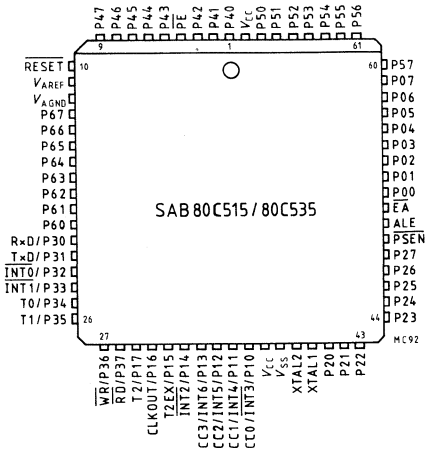
The SAB 80C515/80C535 is a stand-alone, high-performance single-chip microcontroller based on the SAB 8051/80C51 architecture. While maintaining all the SAB 80C51 operating characteristics, the SAB 80C515/80C535 incorporates several enhancements which significantly increase design flexibility and overall system performance.

In addition, the low-power properties of Siemens ACMOS technology allow applications where power consumption and dissipation are critical. Furthermore, the SAB 80C515/80C535 has two software-selectable modes of reduced activity for further power reduction: idle and power-down mode

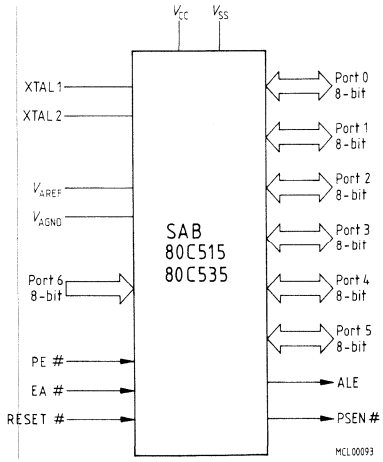
The SAB 80C535 is identical with the SAB 80C515 except that it lacks the on-chip program memory. The SAB 80C515/80C535 is supplied in a 68-pin plastic leaded chip carrier package (PL-CC-68). For the industrial temperature range – 40 to + 85°C, the SAB 80C515/80C535-T40/85 is available.

There are versions for 12 MHz operation and for 16 MHz operation available.

Pin Configuration
(PL-CC-68)



Logic Symbol



Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	I/O	**Port 4** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 4 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors.
PE#	4	I	**Power saving mode enable#** A low level on this pin enables the use of the power saving modes (idle mode and power-down mode). When PE# is held on high level it is impossible to enter the power saving modes.
RESET#	10	I	**Reset pin** A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80C515. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	11		**Reference voltage** for the A/D converter
V_{AGND}	12		**Reference ground** for the A/D converter
P6.7-P6.0	13-20	I	**Port 6** is an 8-bit undirectional input port. Port pins can be used for digital input if voltage levels simultaneously meet the specifications for high/low input voltages and for the eight multiplexed analog inputs of the A/D converter.

Note: Signals signified by an (#) are negated signals.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P3.0-P3.7	21-28	I/O	**Port 3** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 3 pins that have1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – RxD (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – TxD (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) – INT0# (P3.2): interrupt 0 input/timer 0 gate control input – INT1# (P3.3): interrupt 1 input/timer 1 gate control input – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – WR# (P3.6): the write control signal latches the data byte from port 0 into the external data memory – RD# (P3.7): the read control signal enables the external data memory to port 0

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P1.7 - P1.0	29 - 36	I/O	**Port 1** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL} in the DC characteristics) because of the internal pullup resistors. The port is used for the low-order address byte during program verification. Port 1 also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows: – INT3#/CC0 (P1.0): interrupt 3 input/ compare 0 output/capture 0 input – INT4/CC1 (P1.1): interrupt 4 input/ compare 1 output/capture 1 input – INT5/CC2 (P1.2): interrupt 5 input/ compare 2 output/capture 2 input – INT6/CC3 (P1.3): interrupt 6 input/ compare 3 output/capture 3 input – INT2# (P1.4): interrupt 2 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input

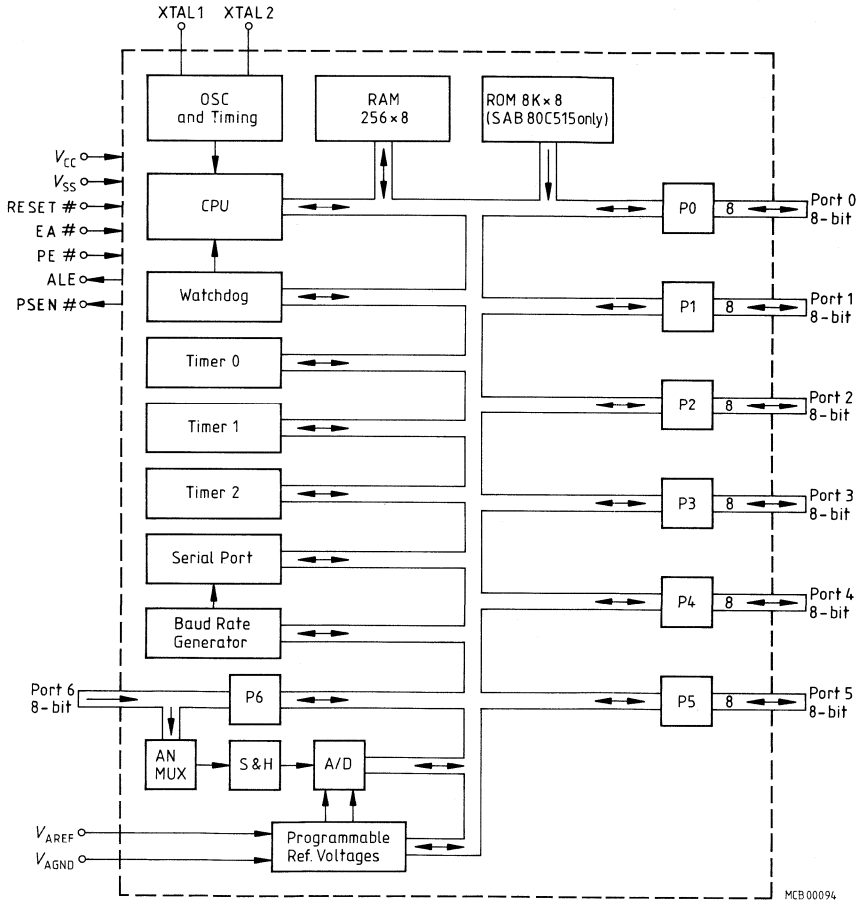
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
XTAL2 XTAL1	39 49		**XTAL2** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. **XTAL1** Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times and rise/fall times specified in the AC characteristics must be observed.
P2.0-P2.7	41- 48	I/O	**Port 2** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application it uses strong internal pullup resistors when issuing 1's. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), port 2 issues the contents of the P2 special function register.
PSEN#	49	O	The **Program store enable#** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. The signal remains high during internal program execution.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
ALE	50	O	The **Address latch enable** output is used for latching the address into external memory during normal operation. It is activated every six oscillator periods, except during an external data memory access.
EA#	51	I	**External access enable#** When held high, the SAB 80C515 executes instructions from the internal ROM as long as the PC is less than 8192. When held low, the SAB 80C515 fetches all instructions from external program memory. For the SAB 80C535 this pin must be tied low.
P0.0-P0.7	42-59	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1's. Port 0 also outputs the code bytes during program verification in the SAB 80C515. External pullup resistors are required during program verification.
P5.7-P5.0	60-67	I/O	**Port 5** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 5 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL} in the DC characteristics) because of the internal pullup resistors.
V_{CC}	37		**Supply voltage** during normal, idle, and power-down operation. Internally connected to pin 68.
V_{SS}	38		**Ground** (0 V)
V_{CC}	68		**Supply voltage** during normal, idle, and power-down operation. Internally connected to pin 37.

Figure 1
Block Diagram



Functional Description

The members of the SAB 80515 family of microcontrollers are:

- SAB 80C515: Microcontroller, designed in Siemens ACMOS technology, with 8 Kbyte factory mask-programmable ROM
- SAB 80C535: ROM-less version of the SAB 80C515
- SAB 80515: Microcontroller, designed in Siemens MYMOS technology, with 8 Kbyte factory mask-programmable ROM
- SAB 80535: ROM-less version of the SAB 80515
- SAB 80515K: Special ROM-less version of the SAB 80515 with an additional interface for program memory accesses. An external ROM that is accessed via the interface substitutes the SAB 80515's internal ROM.

The SAB 80C535 is identical to the SAB 80C515, except that it lacks the on-chip ROM. In this data sheet the term "SAB 80C515" is used to refer to both the SAB 80C515 and SAB 80C535, unless otherwise noted.

Principles of Architecture

The architecture of the SAB 80C515 is based on the SAB 8051/SAB 80C51 microcontroller family. The following features of the SAB 80C515 are fully compatible with the SAB 80C51 features:

- Instruction set
- External memory expansion interface (port 0 and port 2)
- Full-duplex serial port
- Timer/counter 0 and 1
- Alternate functions on port 3
- The lower 128 bytes of internal RAM and the lower 4 Kbytes of internal ROM

The SAB 80C515 additionally contains 128 bytes of internal RAM and 4 Kbytes of internal ROM, which results in a total of 256 bytes of RAM and 8 Kbytes of ROM on-chip.
The SAB 80C515 has a new 16-bit timer/counter with a 2:1 prescaler, reload mode, compare and capture capability. It also contains at 16-bit watchdog timer, an 8-bit A/D converter with programmable reference voltages, two additional quasi-bidirectional 8-bit ports, one 8-bit input port for analog or digital signals, and a programmable clock output ($f_{OSC}/12$).
Furthermore, the SAB 80C515 has a powerful interrupt structure with 12 vectors and 4 programmable priority levels.
Figure 1 shows a block diagram of the SAB 80C515.

CPU

The SAB 80C515 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1.0 µs.

Memory Organization

The SAB 80C515 manipulates operands in the four memory address spaces described below:
Figure 2 illustrates the memory address spaces of the SAB 80C515.

Program Memory

The SAB 80C515 has 8 Kbyte of on-chip ROM, while the SAB 80C535 has no internal ROM. The program memory can be externally expanded up to 64 Kbytes. If the EA# pin is held high, the SAB 80C515 executes out of internal ROM unless the address exceeds 1FFFH. Locations 2000H through 0FFFFH are then fetched from the external program memory. If the EA# pin is held now, the SAB 80C515 fetches all instructions from the external program memory. Since the SAB 80C535 has no internal ROM, pin EA# must be tied low when using this component.

Data Memory

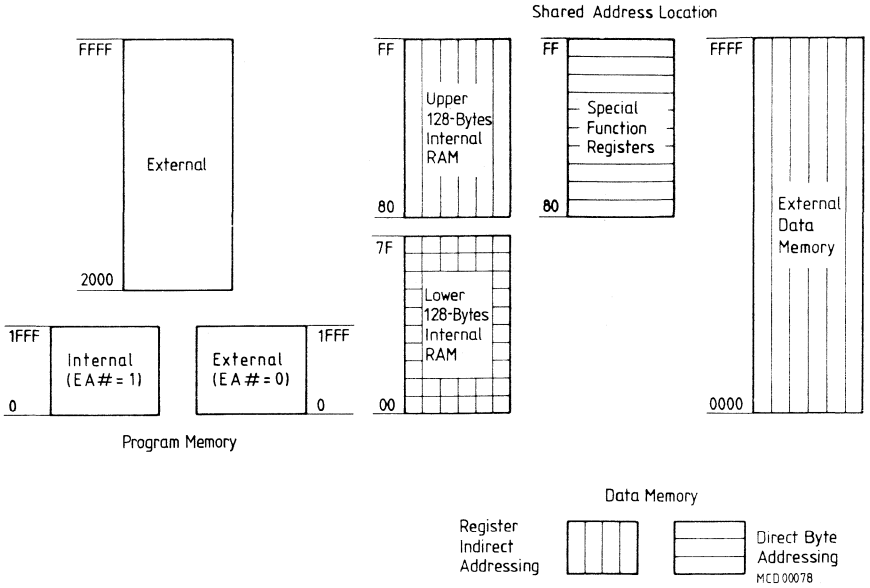
The data memory address space consists of an internal and an external memory space. The internal data memory is divided into three physically separate and distinct blocks: the lower 128 bytes of RAM, the upper 128 bytes of RAM, and the 128 byte special function register (SRF) area. While the upper 128 bytes of data memory and the SFR area share the same address locations, they are accessed through different addressing modes. The lower 128 bytes of data memory can be accessed through direct or register indirect addressing; the upper 128 bytes of RAM can be accessed through register indirect addressing; the special function registers are accessible through direct addressing.
Four 8-register banks, each bank consisting of eight 8-bit multi-purpose registers, occupy locations 0 through 1FH in the lower RAM area. The next 16 bytes, locations 20H through 2FH, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal data memory address space, and the stack depth can be expanded up to 256 bytes.
The external data memory can be expanded up to 64 Kbytes and can be accessed by instructions that use a 16-bit or an 8-bit address.
All registers, except the program counter and the four 8-register banks, reside in the special function register area. The 42 special function registers include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripheral functions. There are also 128 directly addressable bits within the SFR area. The special function registers are listed in table 1.

Table 1
Special Function Register

Symbol	Name	Address
* P0	Port 0	80H
SP	Stack pointer	81H
DPL	Data pointer, low byte	82H
DPH	Data pointer, high byte	83H
PCON	Power control register	87H
* TCON	Timer control register	88H
TMOD	Timer mode register	89H
TL0	Timer 0, low byte	8AH
TL1	Timer 1, low byte	8BH
TH0	Timer 0, high byte	8CH
TH1	Timer 1, high byte	8DH
* P1	Port 1	90H
* SCON	Serial channel control register	98H
SBUF	Serial channel buffer register	99H
* P2	Port 2	0A0H
* IEN0	Interrupt enable register 0	0A8H
IP0	Interrupt priority register 0	0A9H
* P3	Port 3	0B0H
* IEN1	Interrupt enable register 1	0B8H
IP1	Interrupt priority register 1	0B9H
* IRCON	Interrupt request control register	0C0H
CCEN	Compare/capture enable register	0C1H
CCL1	Compare/capture register 1, low byte	0C2H
CCH1	Compare/capture register 1, high byte	0C3H
CCL2	Compare/capture register 2, low byte	0C4H
CCH2	Compare/capture register 2, high byte	0C5H
CCL3	Compare/capture register 3, low byte	0C6H
CCH3	Compare/capture register 3, high byte	0C7H
* T2CON	Timer 2 control register	0C8H
CRCL	Compare/reload/capture register, low byte	0CAH
CRCH	Compare/reload/capture register, high byte	0CBH
TL2	Timer 2, low byte	0CCH
TH2	Timer 2, high byte	0CDH
* PSW	Program status word register	0D0H
* ADCON	A/D converter control register	0D8H
ADDAT	A/D converter data register	0D9H
DAPR	D/A converter program register	0DAH
P6	Port 6	0DBH
* ACC	Accumulator	0E0H
* P4	Port 4	0E8H
* B	B register	0F0H
* P5	Port 5	0F8H

The SFR's marked with an asterisk (*) are bit and byte-addressable.

Figure 2
Memory Address Spaces



I/O Ports

The SAB 80C515 has six 8-bit I/O ports and one 8-bit input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pullup resistors. That means, when configured as inputs, ports 1 to 5 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET. Ports 1 and 3 are provided for several alternate functions, as listed below:

Port	Symbol	Function
P1.0	INT3#/CC0	External interrupt 3 input, compare 0 output, capture 0 input
P1.1	INT4/CC1	External interrupt 4 input, compare 1 output, capture 1 input
P1.2	INT5/CC2	External interrupt 5 input, compare 2 output, capture 2 input
P1.3	INT6/CC3	External interrupt 6 input, compare 3 output, capture 3 input
P1.4	INT2#	External interrupt 2 input
P1.5	T2EX	Timer 2 external reload trigger input
P1.6	CLKOUT	System clock output
P1.7	T2	Timer 2 external reload trigger input
P3.0	RxD	Serial port's receiver data input (asynchronous) or data input/output (synchronous)
P3.1	TxD	Serial port's transmitter data output (asynchronous) or clock output (synchronous)
P3.2	INT0#	External interrupt 0 input, timer 0 gate control
P3.3	INT1#	External interrupt 1 input, timer 1 gate control
P3.4	T0	Timer 0 external counter input
P3.5	T1	Timer 1 external counter input
P3.6	WR#	External data memory write strobe
P3.7	RD#	External data memory read strobe

The SAB 80C515 has dual-purpose input port. As the ANx lines in the SAB 80515 (NMOS version), the eight port lines at port 6 can be used as analog inputs. But if the input voltages at port 6 meet the specified digital input levels (V_{IL} and V_{IH}), the port can also be used as digital input port. Reading the special function register P6 allows the user to input the digital values currently applied to the port pins. It is not necessary to select these modes by software; the voltages applied at port 6 pins can be converted to digital values using the A/D converter and at the same time the pins can be read via SFR P6.
It must be noted, however, that the results in port P6 bits will be indeterminate if the levels at the corresponding pins are not within their respective V_{IL}/V_{IH} specifications.
Furthermore, it is not possible to use port P6 as output lines. Special function register P6 is located at address 0DBH.

Timer/Counters

The SAB 80C515 contains three 16-bit timers/counters which are useful in many applications for timing and counting. The input clock for each timer/counter is 1/12 of the oscillator frequency in the timer operation or can be taken from an external clock source for the counter operation (maximum count rate is 1/24 of the oscillator frequency).

– Timer/Counter 0 and 1

These timers/counters can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto-reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; Timer/counter 1 in this mode holds its count.

External inputs INT0# and INT1# can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

– Timer/Counter 2

Timer/counter 2 of the SAB 80C515 is a 16-bit timer/counter with several additional features. It offers a 2:1 prescaler, a selectable gate function, and compare, capture and reload functions. Corresponding to the 16-bit timer register there are four 16-bit capture/compare registers, one of them can be used to perform a 16-bit reload on a timer overflow or external event. Each of these registers corresponds to a pin of port 1 for capture input/compare output.
Figure 3 shows a block diagram of timer/counter 2.

Reload

A 16-bit reload can be performed with the 16-bit CRC register consisting of CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer 2 overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

Capture

This feature permits saving the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value in timer 2 registers TL2 and TH2 into a dedicated capture register:

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

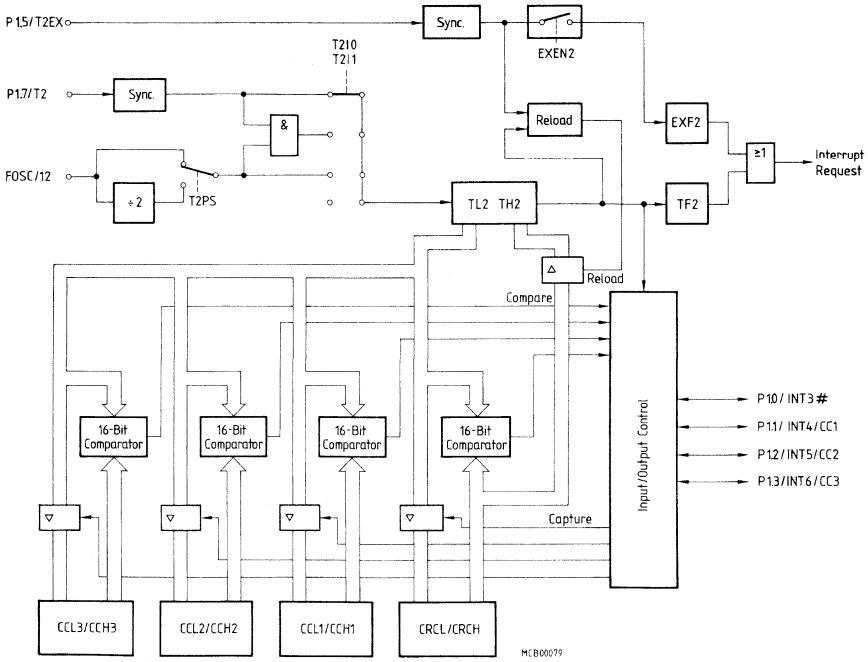
Compare

In the compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 registers. If the count value in the timer 2 registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to a low level when timer 2 overflows.

Mode 1: The transition of the output signal can be determined by software. A timer 2 overflow causes no output change.

Figure 3
Block Diagram of Timer/Counter 2



Serial Port

The serial port of the SAB 80C515 enables full duplex communication between microcontrollers or between microcontroller and peripheral devices.
The serial port can operate in 4 modes:

Mode 0: Shift register mode. Serial data enters and exits through RxD. TxD outputs the shift clock. 8-bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 10-bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). The baud rate is variable.

Mode 2: 11-bits are transmitted (through RxD) or received (through TxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 11-bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Mode 3 is identical to mode 2 except for the baud rate. The baud rate in mode 3 is variable.

The variable baud rates in modes 1 and 3 can be generated by timer 1 or an internal baud rate generator.

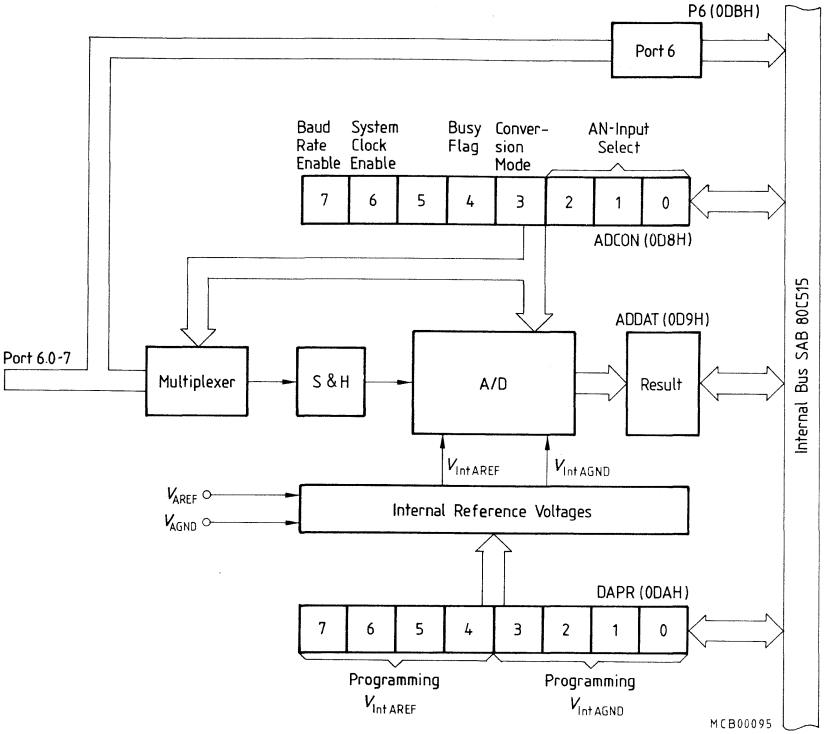
A/D Converter

The 8-bit A/D converter of the SAB 80C515 has eight multiplexed analog inputs (Port 6) and uses the successive approximation method.
There are three characteristic time frames in a conversion cycle (see A/D converter characteristics): the conversion time t_C, which is the time required for one conversion; the sample time t_S which is included in the conversion time and is measured from the start of the conversion; the load time t_L, which in turn is part of the sample time and also is measured from the conversion start.
Within the load time t_L, the analog input capacitance C_I must be loaded to the analog inpult voltage level. For the rest of the sample time t_S, after the load time has passed, the selected analog input must be held constant. During the rest of the conversion time t_C the conversion itself is actually performed. Conversion can be programmed to be single or continuous; at the end of a conversion an interrupt can be generated.

A unique feature is the capability of internal reference voltage programming. The internal reference voltages $V_{IntAREF}$ and $V_{IntAGND}$ for the A/D converter both are programmable to one of 16 steps with respect to the external reference voltages. This feature permits a conversion with a smaller internal reference voltage range to gain a higher resolution. In addition, the internal reference voltages can easily be adapted by software to the desired analog input voltage range.

Figure 4 shows a block diagram of the A/D converter.

Figure 4
Block Diagram of the A/D Converter



Interrupt Structure

The SAB 80C515 has 12 interrupt vectors with the following vector addresses and request flags:

Table 2
Interrupt Sources and Vectors

Source (Request Flags)	Vector	Vector Address
IE0	External interrupt 0	0003H
TF0	Timer 0 interrupt	000BH
IE1	External interrupt 1	0013H
TF1	Timer 1 interrupt	001BH
RI + TI	Serial port interrupt	0023H
TF2 + EXF2	Timer 2 interrupt	002BH
IADC	A/D converter interrupt	0043H
IEX2	External interrupt 2	004BH
IEX3	External interrupt 3	0053H
IEX4	External interrupt 4	005BH
IEX5	External interrupt 5	0063H
IEX6	External interrupt 6	006BH

Each interrupt vector can be individually enabled/disabled. The minimum response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles.

Figure 5 shows the interrupt request sources.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 3 or 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs. Each pair can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1.

Figure 6 shows the priority level structure.

Figure 5
Interrupt Request Sources

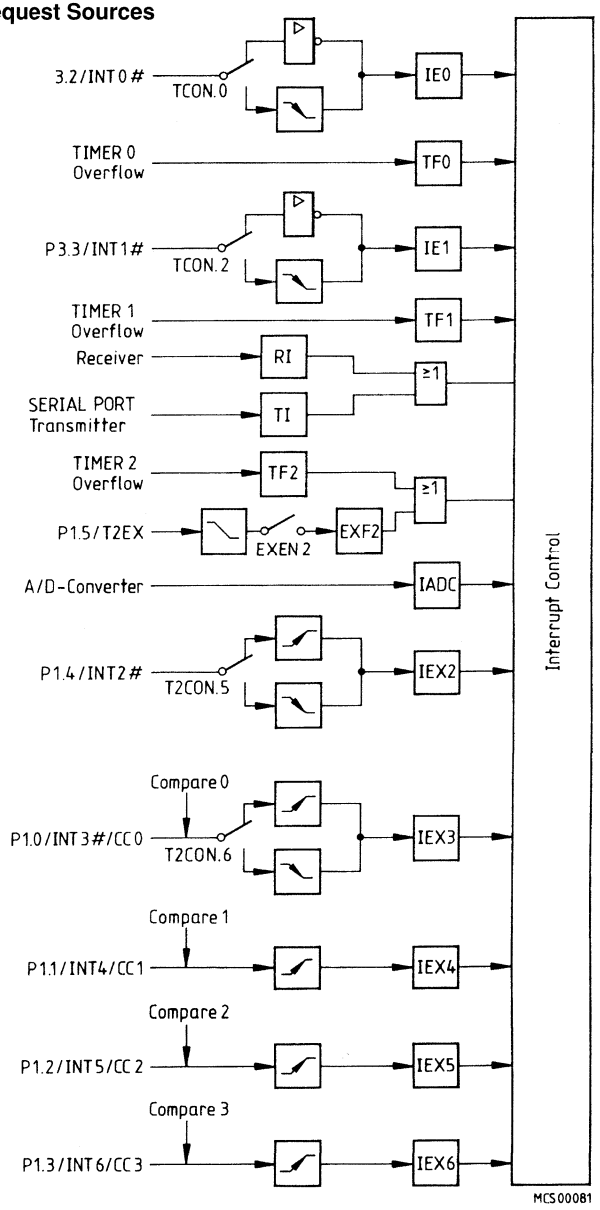
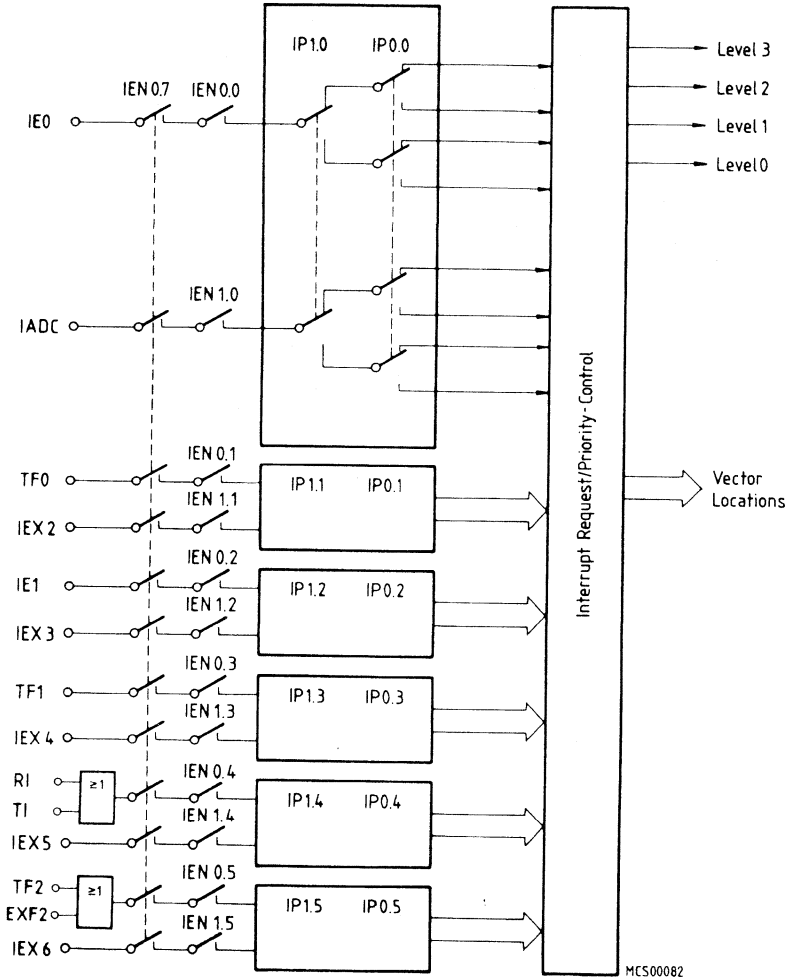


Figure 6
Interrupt Priority Level Structure



Watchdog Timer

This feature is provided as a means of graceful recovery from a software upset. After an external reset, the watchdog timer is cleared and stopped. It can be started and cleared by software, but it cannot be stopped during active mode of the device. If the software fails to clear the watchdog timer at least every 65532 machine cycles (about 65 ms if a 12 MHz oscillator frequency is used), an internal reset will be initiated. The reset cause (external reset or reset caused by the watchdog) can be examined by software. To clear the watchdog, two bits in two different special function registers must be set by two consecutive instructions (bits IEN0.6 and IEN1.6). This is done to prevent the watchdog from being cleared by unexpected opcodes.

It must be noted, however, that the watchdog timer is halted during the idle mode and power-down mode of the processor (see section "Power Saving Modes" below). Therefore, it is possible to use the idle mode in combination with the watchdog timer function. But even the watchdog timer cannot reset the device when one of the power saving modes has been is entered accidentally.
For these reasons several precautions are taken against unintentional entering of the power-down or idle mode (see below).

Power Saving Modes

The ACMOS technology of the SAB 80C515 allows two new power saving modes of the device: The idle mode and the power-down mode. These modes replace the power-down supply mode via pin V_{PD} of the SAB 80515 (NMOS). The SAB 80C515 is supplied via pins V_{CC} also during idle and power-down operation.
However, there are applications where unintentional entering of these power saving modes must be absolutely avoided. Such critical applications often use the watchdog timer to prevent the system from program upsets. Then accidental entering of the power saving modes would even stop the watchdog timer and would circumvent the watchdog timer's task of system protection.

Thus, the SAB 80C515 has an extra pin that allows it to disable both of the power saving modes. When pin PE# is held high, idle mode and power-down mode are completely disabled and the instruction sequences that are used for entering these modes (see below) will NOT affect the normal operations of the device. When PE# is held low, the use of the idle mode and power-down mode is possible as described in the following sections.

Pin PE# has a weak internal pullup resistor. Thus, when left open, the power saving modes are disabled.

The Special Function Register PCON

In the NMOS version SAB 80515 the SFR PCON (address 87H) contains only bit SMOD; in the CMOS version SAB 80C515 there are more bits used (see table 3).

The bits PDE, PDS and IDLE, IDLS select the power-down mode or the idle mode, respectively, when the use of the power saving modes is enabled by pin PE# (see below).

If the power-down mode and the idle mode are set at the same time, power-down takes precedence.

Furthermore, register PCON contains two general purpose flags. For example, the flag bits GF0 and GF1 can be used to give an indication if an interrupt occurred during normal operation or during an idle. Then an instruction that activates Idle can also set one or both flag bits. When idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The reset value of PCON is 000X0000B.

Table 3
SFR PCON (87H)

SMOD	PDS	IDLS	–	GF1	GF0	PDE	IDLE	87H
7	6	5	4	3	2	1	0	

Symbol	Position	Function
SMOD	PCON.7	When set, the baud rate of the serial channel in mode 1, 2, 3 is doubled.
PDS	PCON.6	Power-down start bit. The instruction that sets the PDS flag bit is the last instruction before entering the power-down mode.
IDLS	PCON.5	Idle start bit. The instruction that sets the IDLS flag bit is the last instruction before entering the idle mode.
–	PCON.4	Reserved
GF1	PCON.3	General purpose flag
GF0	PCON.2	General purpose flag
PDE	PCON.1	Power-down enable bit. When set, starting of the power-down mode is enabled.
IDLE	PCON.0	Idle mode enable bit. When set, starting of the idle mode is enabled.

Idle Mode

In the idle mode the oscillator of the SAB 80C515 continues to run, but the CPU is gated off from the clock signal. However, the interrupt system, the serial port, the A/D converter, and all timers with the exception of the watchdog timer are further provided with the clock. The CPU status is preserved in its entirety: the stack pointer, program counter, program status word, accumulator, and all other registers maintain their data during idle mode.

The reduction of power consumption, which can be achieved by this feature depends on the number of peripherals running.

If all timers are stopped and the A/D converter and the serial interface are not running, the maximum power reduction can be achieved. This state is also the test condition for the idle mode I_{CC} (see DC characteristics, note 5).

So the user has to take care which peripheral should continue to run and which has to be stopped during idle mode. Also the state of all port pins – either the pins controlled by their latches or controlled by their secondary functions – depends on the status of the controller when entering idle mode.

Normally the port pins hold the logical state they had at the time idle mode was activated. If some pins are programmed to serve their alternate functions they still continue to output during idle mode if the assigned function is on. This applies to the compare outputs as well as to the clock output signal or to the serial interface in case it cannot finish reception or transmission during normal operation. The control signals ALE and PSEN# hold at logic high levels (see table 4).

Table 4
Status of External Pins During Idle and Power-Down Mode

	Last instruction executed from internal code memory		Last instruction executed from external code memory	
Outputs	**Idle**	**Power-down**	**Idle**	**Power-down**
ALE	High	Low	High	Low
PSEN	High	Low	High	Low
PORT 0	Data	Data	Float	Float
PORT 1	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output
PORT 2	Data	Data	Address	Data
PORT 3	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output
PORT 4	Data	Data	Data	Data
PORT 5	Data	Data	Data	Data

As in normal operation mode, the ports can be used as inputs during idle mode. Thus a capture or reload operation can be triggered, the timers can be used to count external events, and external interrupts will be detected.

The idle mode is a useful feature which makes it possible to "freeze" the processor's status – either for a predefined time, or until an external event reverts the controller to normal operation, as discussed below. The watchdog timer is the only peripheral which is automatically stopped during idle mode. If it were not disabled on entering idle mode, the watchdog timer would reset the controller, thus abandoning the idle mode.

When idle mode is used, pin PE# must be held on low level. The idle mode is then entered by two consecutive instructions. The first instruction sets the flag bit IDLE (PCON.0) and must not set bit IDLS (PCON.5), the following instruction sets the start bit IDLS (PCON.5) and must not set bit IDLE (PCON.0). The hardware ensures that a concurrent setting of both bits, IDLE and IDLS, does not initiate the idle mode. Bits IDLE and IDLS will automatically be cleared after being set. If one of these register bits is read the value that appears is 0 (see table 3). This double instruction is implemented to minimize the chance of an unintentional entering of the idle mode which would leave the watchdog timer's task of system protection without effect.

Note that PCON is not a bit-addressable register, so the above mentioned sequence for entering the idle mode is obtained by byte-handling instructions, as shown in the following example:

```
ORL     PCON,#00000001B   ;Set bit IDLE, bit IDLS must not be set
ORL     PCON,#00100000B   ;Set bit IDLS, bit IDLE must not be set
```

The instruction that sets bit IDLS is the last instruction executed before going into idle mode.

There are two ways to terminate the idle mode:

- The idle mode can be terminated by activating any enable interrupt. This interrupt will be serviced and normally the instruction to be executed following the RETI instruction will be the one following the instruction that sets the bit IDLS.
- The other way to terminate the idle mode, is a hardware reset. Since the oscillator is still running, the hardware reset must be held active only for two machine cycles for a complete reset.

Power-Down Mode

In the power-down mode, the on-chip oscillator is stopped. Therefore all functions are stopped; only the contents of the on-chip RAM and the SFR's are maintained.The port pins controlled by their port latches output the values that are held by their SFR's.
The port pins which serve the alternate output functions show the values they had at the end of the last cycle of the instruction which initiated the power-down mode; when the clockout signal (CLKOUT, P1.6) is enabled, it will stop at low level. ALE and PSEN# hold at logic low level (see table 4).

To enter the power-down mode the pin PE# must be on low level. The power-down mode then is entered by two consecutive instructions. The first instruction has to set the flag bit PDE (PCON.1) and must not set bit PDS (PCON.6), the following instruction has to set the start bit PDS (PCON.6) and must not set bit PDE (PCON.1). The hardware ensures that a concurrent setting of both bits, PDE and PDS, does not initiate the power-down mode. Bits PDE and PDS will automatically be cleared after having been set and the value shown by reading one of these bits is always 0 (see table 3). This double instruction is implemented to minimize the chance of unintentionally entering the power-down mode which could possibly "freeze" the chip's activity in an undesired status.

Note that PCON is not a bit-addressable register, so the above mentioned sequence for entering the power-down mode is obtained by byte-handling instructions, as shown in the following example:

```
ORL     PCON,#00000010B   ;Set bit PDE, bit PDS must not be set
ORL     PCON,#01000000B   ;Set bit PDS, bit PDE must not be set
```

The instruction that sets bit PDS is the last instruction executed before going into power-down mode.

The only exit from power-down mode is a hardware reset. Reset will redefine all SFR's, but will not change the contents of the internal RAM.

In the power-down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the power- down mode is invoked, and that V_{CC} is restored to its normal operating level, before the power-down mode is terminated. The reset signal that terminates the power-down mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (similar to power-on reset).

Differences in Pin Assignments of the SAB 80C515 and SAB 80515

Since the SAB 80C515 is designed in CMOS technology, this device requires no V_{BB} pin, because the die's substrate is internally connected to V_{CC}.

Furthermore, the RAM backup power supply via pin V_{PD} is replaced by the software-controlled power-down mode and power supply via V_{CC}.

Therefore, pins V_{BB} and V_{PD} of the NMOS version SAB 80515 are used for other functions in the SAB 80C515.

Pin 4 (the former pin V_{PD}) is the new PE# pin which enables the use of the power saving modes.

Pin 37 (the former pin V_{BB}) becomes an additional V_{CC} pin. Thus, it is possible to insert a decoupling capacitor between pin 37 (V_{CC}) and pin 38 (V_{SS}) very close to the device, thereby avoiding long wiring and reducing the voltage distortion resulting from high dynamic current peaks.

There is a difference between the NMOS and CMOS version concerning the clock circuitry. When the device is driven from an external source, pin XTAL2 must be driven by the clock signal; pin XTAL1, however, must be left open in the SAB 80C515 (must be tied low in the NMOS version). When using the oscillator with a crystal there is no difference in the circuitry.

Thus, due to its pin compatibility the SAB 80C515 normally substitutes any SAB 80515 without redesign of the user's printed circuit board, but the user has to take care that the two V_{CC} pins are hardwired on-chip. In any case, it is recommended that power is supplied on both V_{CC} pins of the SAB 80C515 to improve the power supply to the chip.
If the power saving modes are to be used, pin PE# must be tied low, otherwise these modes are disabled.

Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct*)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accu	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accu	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accu	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Notes on data addressing modes:

Rn – Working register R0 – R7

direct – 128 internal RAM locations, any I/O port, control or status register

@Ri – Indirect internal or external RAM location addressed by register R0 or R1

#data – 8-bit constant included in instruction

#data 16 – 16-bit constant included as bytes 2 and 3 of instruction

bit – 128 software flags, any I/O pin, control or status bit

A – Accumulator

Notes on program addressing modes

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.

addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.

rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is + 127/– 128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr,code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr,code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,*#data*
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr,code addr*
31	2	ACALL	*code addr*
32	1	RETI	

Hex code	Number of bytes	Mnemonic	Operands
33	1	RLC	A
34	2	ADDC	A,*#data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr,#data*
44	2	ORL	A,*#data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr,#data*
54	2	ANL	A,*#data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr,#data*
64	2	XRL	A,*#data*
65	2	XRL	A,*data addr*

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
66	1	XRL	A,@R0
67	1	XRL	A,@R1
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr*,*data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*,R2
8B	2	MOV	*data addr*,R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data*,*code addr*
B5	3	CJNE	A,*data addr*,*code addr*
B6	3	CJNE	@R0,#*data*,*code addr*
B7	3	CJNE	@R1,#*data*,*code addr*
B8	3	CJNE	R0,#*data*,*code addr*
B9	3	CJNE	R1,#*data*,*code addr*
BA	3	CJNE	R2,#*data*,*code addr*
BB	3	CJNE	R3,#*data*,*code addr*
BC	3	CJNE	R4,#*data*,*code addr*
BD	3	CJNE	R5,#*data*,*code addr*
BE	3	CJNE	R6,#*data*,*code addr*
BF	3	CJNE	R7,#*data*,*code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr**)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr*,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	0 to + 70°C (SAB 80C515)
	– 40 to + 85°C (SAB 80C515-T40/85)
	– 40 to + 110°C (SAB 80C515-T40/110)
Storage temperature	– 65 to + 150°C
Voltage on any pin with respect to ground (V_{SS})	– 0.5 to V_{CC} + 0.5 V
Voltage on V_{CC} to V_{SS}	– 0.5 to + 6.5 V
Power dissipation	2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V; T_A = 0 to + 70°C; for SAB 80C515/80C535
T_A = – 40 to + 85°C for SAB 80C515/80C535-T40/85
T_A = – 40 to + 110°C for SAB 80C515/80C535-T40/110

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except EA#)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage (EA#)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input high voltage (except RESET# and XTAL2)	V_{IH}	2.0 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL2	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	–
Input high voltage to RESET#	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage, ports 1, 2, 3, 4, 5	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA 1)
Output low voltage, port 0, ALE, PSEN#	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA 1)
Output high voltage, ports 1, 2, 3, 4, 5	V_{OH}	2.4 0.9 V_{CC}	– –	V V	I_{OH} = – 80 µA I_{OH} = – 10 µA
Output high voltage (port 0 in external bus mode, ALE, PSEN)	V_{OH1}	2.4 0.9 V_{CC}	– –	V V	I_{OH} = – 400 µA I_{OH} = – 40 µA 2)
Logic 0 input current, ports 1, 2, 3, 4, 5	I_{IL}	–	– 50	µA	V_{IN} = 0.45 V

for notes see next page

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Output high voltage (port 0 in external bus mode, ALE PSEN)	V_{OH1}	2.4 0.9 V_{CC}	– –	V	$I_{OH} = -400$ µA $I_{OH} = -40$ µA [2]
Logic 0 input current, ports 1, 2, 3, 4, 5,	I_{IL}	–	– 50	µA	$V_{IN} = 0.45$ V
Input low current to RESET# for reset	I_{IL2}	–	– 100	µA	$V_{IN} = 0.45$ V
Logical 1-to-0 transition current, ports 1, 2, 3, 4, 5	I_{TL}	–	– 650	µA	$V_{IN} = 2$ V
Input leakage current (port 0, EA#)	I_{LI}	–	± 10	µA	$0.45 < V_{IN} < V_{CC}$
Pin capacitance	C_{IO}	–	10	pF	$f_C = 1$ MHz, $T_A = 25$°C
Power-supply current:					
Active mode, 12 MHz [6]	–	–	35	mA	$V_{CC} = 5$ V [4]
Idle mode, 12 MHz [6]	–	–	13	mA	$V_{CC} = 5$ V [5]
Active mode, 16 MHz [6]	–	–	46	mA	$V_{CC} = 5$ V [4]
Idle mode, 16 MHz [6]	–	–	17	mA	$V_{CC} = 5$ V [5]
Power-down mode	–	–	50	µA	$V_{CC} = 2$ V to 5.5 V [3]

Notes

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1, 3, 4 and 5. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation.
In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V.
Then, it may be desirable to qualify ALE with a Schmitttrigger, or use an address latch with a Schmitttrigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the VOH on ALE and PSEN to momentarily fall below the 0.9 V_{CC} specification when the address bits are stabilizing.

3) Power-down I_{CC} is measured with: EA# = Port 0 = Port 6 = V_{CC};
XTAL1 = N.C.; XTAL2 = V_{SS}; RESET# = V_{CC}; $V_{AGND} = V_{SS}$; all other pins are disconnected.

4) I_{CC} (active mode) is measured with: XTAL2 driven with the clock signal according to the figure below; XTAL1 = N.C.; EA# = Port 0 = Port 6 = V_{CC}; RESET# = V_{SS}; all other pins are disconnected. I_{CC} might be slightly higher if a crystal oscillator is used.

5) I_{CC} (idle mode) is measured with: XTAL2 driven with the clock signal according to the figure below; XTAL1 = N.C.; EA# = V_{SS}; Port 0 = Port 6 V_{CC}; RESET# = V_{CC}; all other pins are disconnected; all on-chip peripherals are disabled.

6) I_{CC} at other frequencies is given by:
Active mode: $I_{CC\ max}$ (mA) = 2.67 × f_{OSC} (MHz) + 3.00
Idle mode: $I_{CC\ max}$ (mA) = 0.88 × f_{OSC} (MHz) + 2.50
where f_{OSC} is the oscillator frequency in MHz.
$I_{CC\ max}$ is given in mA and measured at V_{CC} = 5 V (see also notes 4 and 5)

A/D Converter Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V; V_{AREF} = V_{CC} ± 5%; V_{AGND} = V_{SS} ± 0.2 V;
$V_{IntAREF} - V_{IntAGND} \geq 1$ V; T_A = 0 to + 70°C for SAB 80C515/80C535
T_A = – 40 to + 85°C for SAB 80C515/80C535-T40/85
T_A = – 40 to + 110°C for SAB 80C515/80C535-T40/110

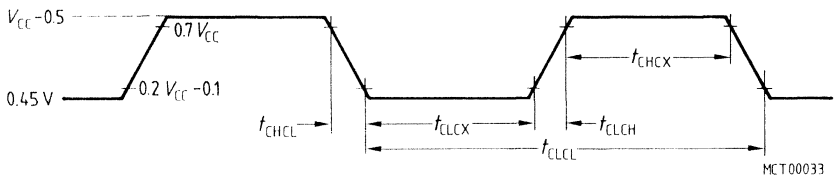
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Analog input voltage	V_{AINPUT}	V_{AGND} – 0.2	–	V_{AREF} + 0.2	V	9)
Analog input capacitance	C_I	–	25	45	pF	7)
Load time	t_L	–	–	2 t_{CY}	µs	–
Sample time (incl. load time)	t_S	–	–	7 t_{CY}	µs	–
Conversion time (incl. sample time)	t_C	–	–	13 t_{CY}	µs	–
Differential non-linearity	DNLE	–	± 1/2	± 1	LSB	$V_{IntAREF}$ =
Integral non-linearity	INLE	–	± 1/2	± 1	LSB	V_{AREF} = V_{CC}
Offset error			± 1/2	± 1	LSB	$V_{IntAGND}$ =
Gain error			± 1/2	± 1	LSB	V_{AGND} = V_{SS}
Total unadjusted error	TUE		± 1	± 2	LSB	7)
V_{AREF} supply current	I_{REF}	–	–	5	mA	8)
Internal reference error	$V_{IntREFERR}$	–	–	TBD	mV	8)

7) The output impedance of the analog source must be low enough to assure full loading of the sample capacitance (C_I) during load time (t_L). After charging of the internal capacitance (C_I) in the load time (t_L) the analog input must be held constant for the rest of the sample time (t_S).

8) The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

9) Exceeding these limit values at one or more input channels will cause additional current which is sinked / sourced at these channels. This may also affect the accuracy of other channels which are operated within these specifications.

Clock Signal Waveform for I_{CC} Tests in Active and Idle Mode
(t_{CLCH} = t_{CHCL} = 5 ns)



AC Characteristics for SAB 80C515/80C535

V_{CC} = 5 V ± 10%; V_{SS} = 0 V (C_L for Port 0, ALE and PSEN# outputs = 100 pF; C_L for all outputs = 80 pF) T_A = 0 to + 70°C for SAB 80C515/80C535
T_A = – 40 to + 85°C for SAB 80C515/80C535-T40/85
T_A = – 40 to + 110°C for SAB 80C515/80C535-T40/110

Parameter	Symbol	Limit Values				Unit
		12 MHz clock		Variable clock 1/ t_{CLCL} = 0.5 to 12 MHz		
		min.	max	min.	max.	
Program Memory Characteristics						
ALE pulse width	t_{LHLL}	127	–	2 t_{CLCL} – 40	–	ns
Address setup to ALE	t_{AVLL}	53	–	t_{CLCL} – 30	–	ns
Address hold after ALE	t_{LLAX}	48	–	t_{CLCL} – 35	–	ns
ALE to valid instruction in	t_{LLIV}	–	233	–	4 t_{CLCL} – 100	ns
ALE to PSEN#	t_{LLPL}	58	–	t_{CLCL} – 25	–	ns
PSEN# pulse width	t_{PLPH}	215		3 t_{CLCL} – 35		ns
PSEN# to valid instruction in	t_{PLIV}	–	150	–	3 t_{CLCLL} – 100	ns
Input instruction hold after PSEN#	t_{PXIX}	0	–	0	–	ns
Input instruction float after PSEN#	t_{PXIZ} [1]	–	63	–	t_{CLCL} – 20	ns
Address valid after PSEN#	t_{PXAV} [1]	75		t_{CLCL} – 8		ns
Address to valid instruction in	t_{AVIV}	–	302	–	5 t_{CLCLL} – 115	ns
Address float to PSEN#	t_{AZPL}	0	–	0	–	ns

[1] Interfacing the SAB 80C515 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for SAB 80C515/80C535 (cont'd)

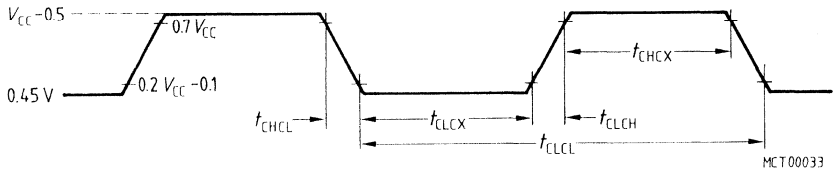
V_{CC} = 5 V ± 10%; V_{SS} = 0 V (C_L for Port 0, ALE and PSEN# outputs = 100 pF; C_L for all outputs = 80 pF)
T_A = 0 to + 70°C for SAB 80C515/80C535
T_A = – 40 to + 85°C for SAB 80C515/80C535-T40/85
T_A = – 40 to + 110°C for SAB 80C515/80C535-T40/110

Parameter	Symbol	Limit Values				Unit
		12 MHz clock		Variable clock 1/ t_{CLCL} = 0.5 to 12 MHz		
		min.	max	min.	max.	
External Data Memory Characteristics						
RD# pulse width	t_{RLRH}	400	–	6 t_{CLCL} – 100	–	ns
WR# pulse width	t_{WLWH}	400	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	132	–	2 t_{CLCL} – 35	–	ns
RD# to valid data in	t_{RLDV}	–	252	–	5 t_{CLCL} – 165	ns
DATA hold after RD#	t_{RHDX}	0	–	0		ns
Data float after RD#	t_{RHDZ}	–	97	–	2 t_{CLCL} – 70	ns
ALE to valid data in	t_{LLDV}	–	517	–	8 t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	585	–	9 t_{CLCL} – 165	ns
ALE to WR# or RD#	t_{LLWL}	200	300	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
WR# or RD# high to ALE high	t_{WHLH}	43	123	t_{CLCL} – 40	t_{CLCL} + 40	ns
Address valid to WR#	t_{AVWL}	203	–	4 t_{CLCL} – 130	–	ns
Data valid to WR# transition	t_{QVWX}	33	–	t_{CLCL} – 50	–	ns
Data setup before WR#	t_{QVWH}	433	–	7 t_{CLCL} – 150	–	ns
Data hold after WR#	t_{WHQX}	33	–	t_{CLCL} – 50	–	ns
Address float after RD#	t_{RLAZ}	–	0	–	0	ns

AC Characteristics for SAB 80C515/80C535 (cont'd)

Parameter	Symbol	Limit Values		Unit
		Variable clock Frequ. = 0.5 to 12 MHz		
		min.	max.	
External Clock Drive				
Oscillator period	t_{CLCL}	83.3	2000	ns
Oscillator frequency	$1/t_{CLCL}$	0.5	12	MHz
High time	t_{CHCX}	20	–	ns
Low time	t_{CLCX}	20	–	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns

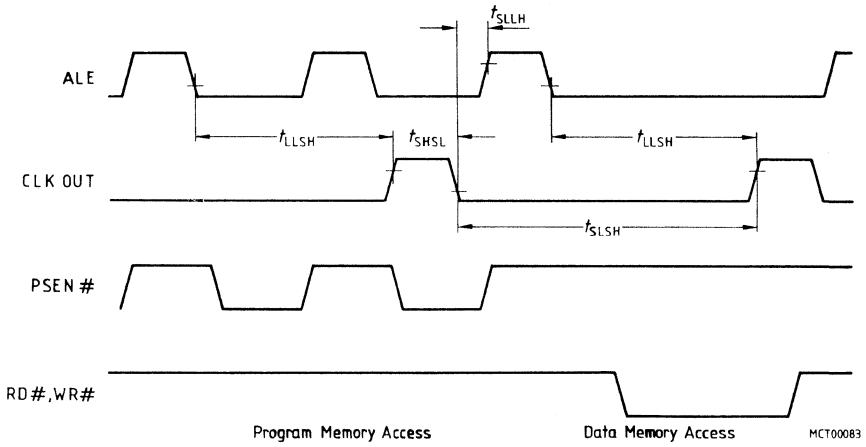
External Clock Cycle



System Clock Timing for SAB 80C515/80C535

Parameter	Symbol	Limit Values				Unit
		12 MHz clock		Variable clock 1/ f_{CLCL} = 0.5 to 12 MHz		
		min.	max	min.	max.	
ALE to CLKOUT	t_{LLSH}	543	–	7 t_{CLCL} – 40	–	ns
CLKOUT high time	t_{SHSL}	127	–	2 t_{CLCL} – 40	–	ns
CLKOUT low time	t_{SLSH}	793	–	10 t_{CLCL} – 40	–	ns
CLKOUT low to ALE high	t_{SLLH}	43	123	t_{CLCL} – 40	t_{CLCL} +40	ns

System Clock Timing



AC Characteristics for SAB 80C515-16/80C535-16

V_{CC} = 5 V ± 10%; V_{SS} = 0 V (C_L for Port 0, ALE and PSEN# outputs = 100 pF; C_L for all outputs = 80 pF) T_A = 0 to + 70°C for SAB 80C515-16/80C535-16
T_A = – 40 to + 85°C for SAB 80C515-16/80C535-16-T40/85

Parameter	Symbol	Limit Values				Unit
		16 MHz clock		Variable clock 1/ t_{CLCL} = 0.5 to 16 MHz		
		min.	max	min.	max.	
Program Memory Characteristics						
ALE pulse width	t_{LHLL}	85	–	2 t_{CLCL} – 40	–	ns
Address setup to ALE	t_{AVLL}	33	–	t_{CLCL} – 30	–	ns
Address hold after ALE	t_{LLAX}	28	–	t_{CLCL} – 35	–	ns
ALE to valid instruction in	t_{LLIV}	–	150	–	4 t_{CLCL} – 100	ns
ALE to PSEN#	t_{LLPL}	38	–	t_{CLCL} – 25	–	ns
PSEN# pulse width	t_{PLPH}	153		3 t_{CLCL} – 35		ns
PSEN# to valid instruction in	t_{PLIV}	–	88	–	3 t_{CLCLL} – 100	ns
Input instruction hold after PSEN#	t_{PXIX}	0	–	0	–	ns
Input instruction float after PSEN#	t_{PXIZ} [1]	–	48	–	t_{CLCL} – 20	ns
Address valid after PSEN#	t_{PXAV} [1]	60		t_{CLCL} – 8		ns
Address to valid instruction in	t_{AVIV}	–	223	–	5 t_{CLCLL} – 115	ns
Address float to PSEN#	t_{AZPL}	0	–	0	–	ns

[1] Interfacing the SAB 80C515-16 to devices with float times up to 55 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for SAB 80C515-16/80C535-16 (cont'd)

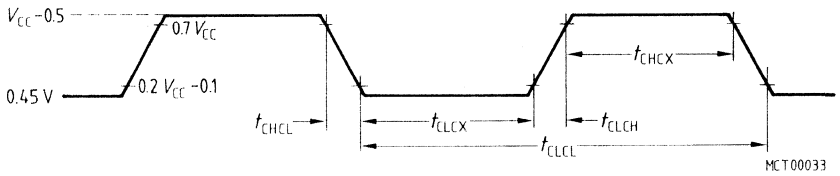
V_{CC} = 5 V ± 10%; V_{SS} = 0 V (C_L for Port 0, ALE and PSEN# outputs = 100 pF; C_L for all outputs = 80 pF) T_A = 0 to +70°C for SAB 80C515-16/80C535-16
T_A = – 40 to + 85°C for SAB 80C515-16/80C535-16-T40/85

Parameter	Symbol	Limit Values				Unit
		16 MHz clock		Variable clock 1/ t_{CLCL} = 0.5 to 16 MHz		
		min.	max	min.	max.	
External Data Memory Characteristics						
RD# pulse width	t_{RLRH}	275	–	6 t_{CLCL} – 100	–	ns
WR# pulse width	t_{WLWH}	275	–	6 t_{CLCL} – 100	–	ns
Address hold after ALE	t_{LLAX2}	90	–	2 t_{CLCL} – 35	–	ns
RD# to valid data in	t_{RLDV}	–	148	–	5 t_{CLCL} – 165	ns
DATA hold after RD#	t_{RHDX}	0	–	0		ns
Data float after RD#	t_{RHDZ}	–	55	–	2 t_{CLCL} – 70	ns
ALE to valid data in	t_{LLDV}	–	350	–	8 t_{CLCL} – 150	ns
Address to valid data in	t_{AVDV}	–	398	–	9 t_{CLCL} – 165	ns
ALE to WR# or RD#	t_{LLWL}	138	238	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
WR# or RD# high to ALE high	t_{WHLH}	23	103	t_{CLCL} – 40	t_{CLCL} + 40	ns
Address valid to WR#	t_{AVWL}	120	–	4 t_{CLCL} – 130	–	ns
Data valid to WR# transition	t_{QVWX}	13	–	t_{CLCL} – 50	–	ns
Data setup before WR#	t_{QVWH}	288	–	7 t_{CLCL} – 150	–	ns
Data hold after WR#	t_{WHQX}	13	–	t_{CLCL} – 50	–	ns
Address float after RD#	t_{RLAZ}	–	0	–	0	ns

AC Characteristics for SAB 80C515-16/80C535-16 (cont'd)

Parameter	Symbol	Limit Values		Unit
		Variable clock Frequ. = 0.5 to 16 MHz		
		min.	max.	
External Clock Drive				
Oscillator period	t_{CLCL}	62.5	2000	ns
Oscillator frequency	$1/t_{CLCL}$	0.5	16	MHz
High time	t_{CHCX}	15	–	ns
Low time	t_{CLCX}	15	–	ns
Rise time	t_{CLCH}	–	15	ns
Fall time	t_{CHCL}	–	15	ns

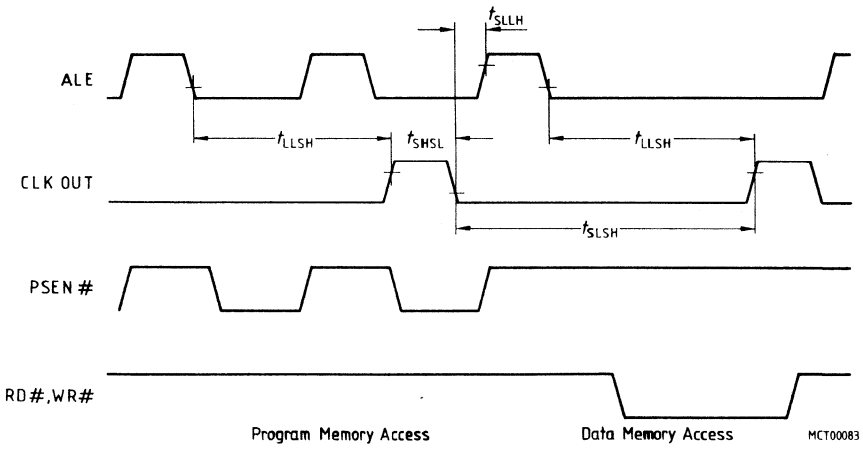
External Clock Cycle



System Clock Timing for SAB 80C515-16/80C535-16

Parameter	Symbol	Limit Values				Unit
		16 MHz clock		Variable clock 1/ t_{CLCL} = 0.5 to 16 MHz		
		min.	max	min.	max.	
ALE to CLKOUT	t_{LLSH}	398	–	7 t_{CLCL} – 40	–	ns
CLKOUT high time	t_{SHSL}	85	–	2 t_{CLCL} – 40	–	ns
CLKOUT low time	t_{SLSH}	585	–	10 t_{CLCL} – 40	–	ns
CLKOUT low to ALE high	t_{SLLH}	23	103	t_{CLCL} – 40	t_{CLCL} + 40	ns

System Clock Timing

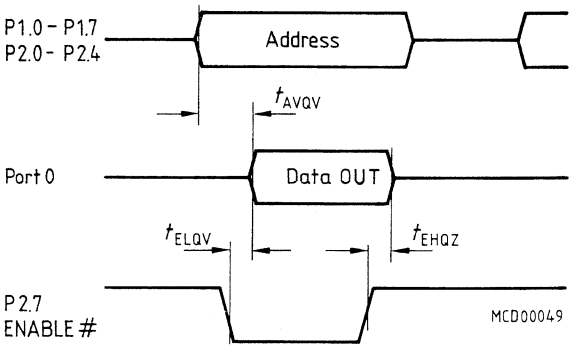


ROM Verification Characteristics

T_A = 25°C ± 5°C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	$48t_{CLCL}$	ns
ENABLE to valid data	t_{ELQV}	–	$48t_{CLCL}$	ns
Data float after ENABLE	t_{EHQZ}	0	$48t_{CLCL}$	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz

ROM Verification



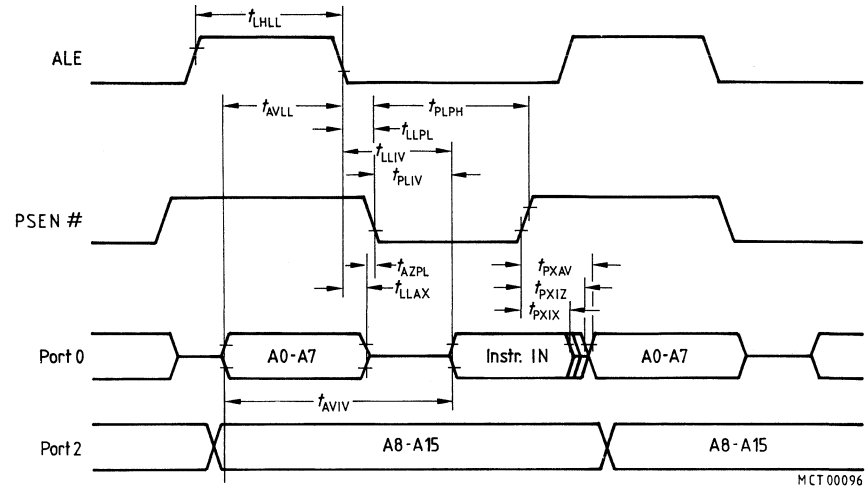
Address: P1.0–P1.7 = A0–A7
P2.0–P2.4 = A8–A12

Data: Port 0 = D0–D7

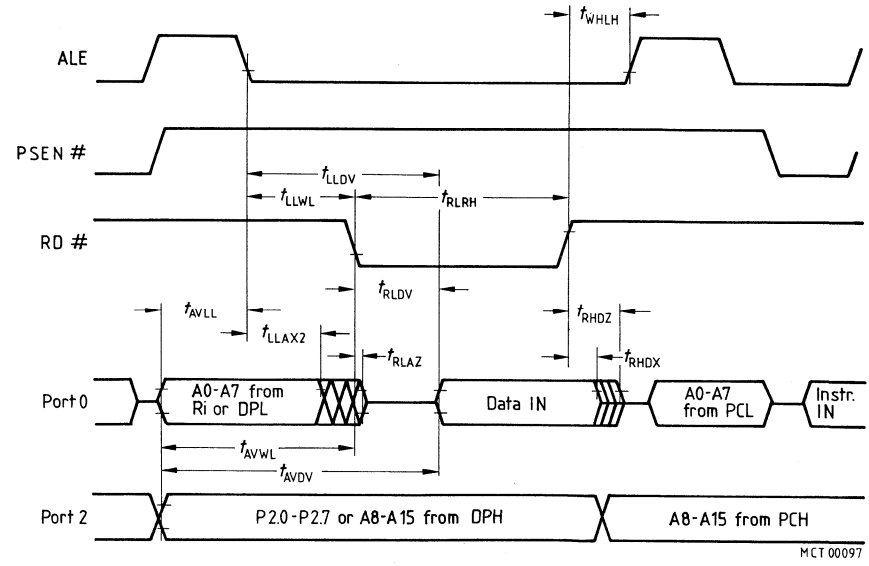
Inputs: P2.5–P2.6, PSEN# = V_{SS}
ALE, EA# = V_{IH}
RESET# = V_{IH1}

Waveforms

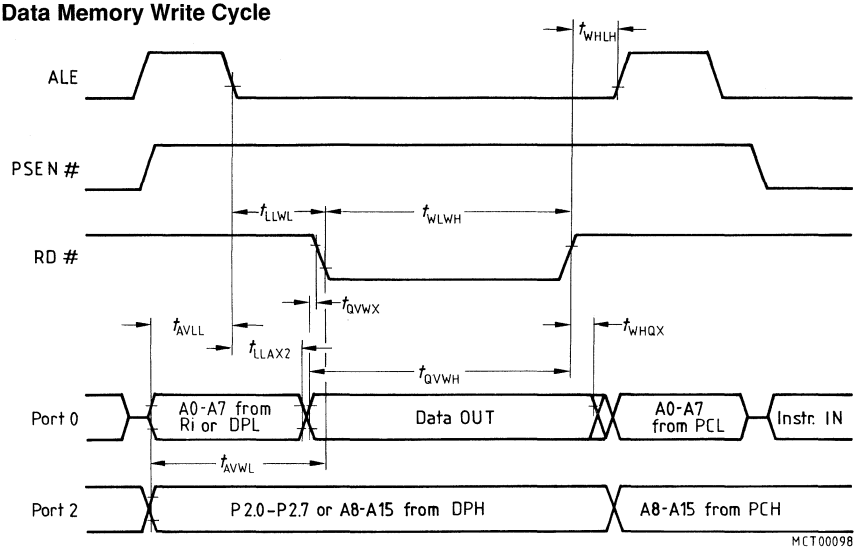
Program Memory Read Cycle



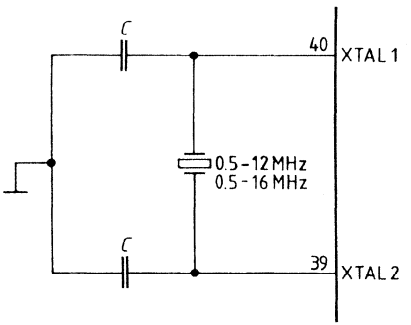
Data Memory Read Cycle



Data Memory Write Cycle

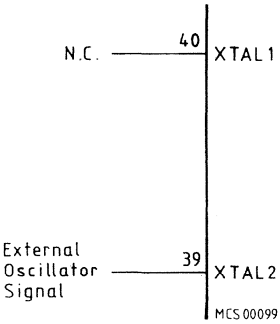


Recommended Oscillator Circuits



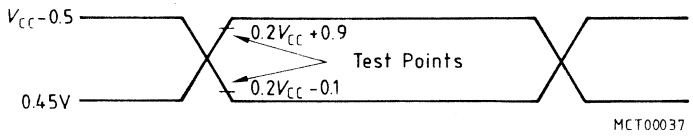
C = 30 pF ± 10 pF
(incl. stray capacitance)

Crystal Oscillator Mode



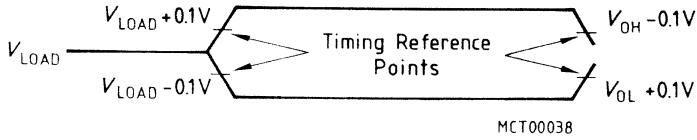
Driving from External Source

AC Testing: Input, Output Waveforms



AC inputs during testing are driven at V_{CC} – 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at $V_{IH\ min}$ for a logic '1' and $V_{IL\ max}$ for a logic '0'.

AC Testing: Float Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV deviation from the load voltage V_{OH}/V_{OL} occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

SIEMENS

High-Performance 8-Bit CMOS Single-Chip Microcontroller

SAB 80C517/80C537
SAB 80C517-16/80C537-16

Advanced Information

SAB 80C517 Microcontroller with factory mask-programmable ROM
SAB 80C537 Microcontroller for external ROM

- SAB 80C517/80C537, 12 MHz operation
- SAB 80C517-16/80C537-16, 16 MHz operation
- 8 K × 8 ROM (SAB 80C517 only)
- 256 × 8 on-chip RAM
- Superset of SAB 80C51 architecture:
  - 1 µs instruction cycle time at 12 MHz
  - 750 ns instruction cycle time art 16 MHz
  - 256 directly addressable bits
  - Boolean processor
  - 64 Kbyte external data and program memory addressing
- Four 16-bit timer/counters
- Powerful 16-bit compare/capture unit (CCU) with up to 21 high-speed or PWM output channels and 5 capture inputs
- Versatile "fail-safe" provisions
- Fast 32-bit division, 16-bit 2 multiplication, 32-bit normalize and shift by peripheral MUL/DIV unit (MDU)
- Eight data pointers for external memory addressing
- Fourteen interrupt vectors, four priority levels selectable
- 8-bit A/D converter with 12 multiplexed inputs and programmable ref. voltages
- Two full duplex serial interfaces
- Fully upward compatible with SAB 80C515
- Extended power saving modes
- Nine ports: 56 I/O lines, 12 input lines
- Three temperature ranges available:
  0 to 70°C
  – 40 to 85°C
  – 40 to 110°C
- Plastic package: PL-CC-84, P-QFP-100

Ordering Information

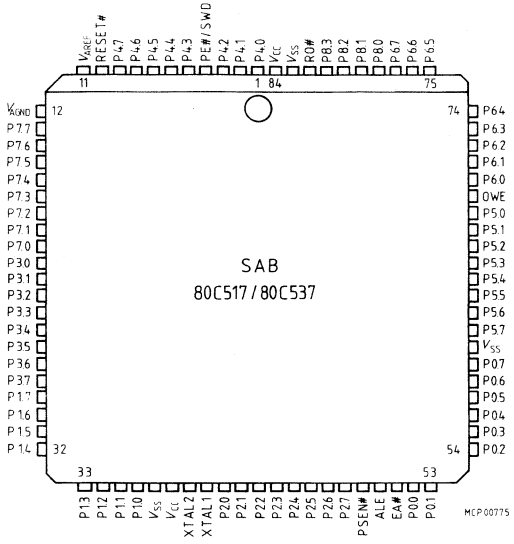
Type	Ordering code	Package	**Description** (8-bit CMOS microcontroller)
SAB 80C517-N	Q67120-C397	PL-CC-84	with factory mask-programmable ROM, 12 MHz
SAB 80C537-N	Q67120-C452	PL-CC-84	for external memory, 12 MHz
SAB 80C517-N-T40/85	Q67120-C483	PL-CC-84	with factory mask-programmable ROM, 12 MHz, ext. temperature – 40 to + 85 °C
SAB 80C537-N-T40/85	Q67120-C484	PL-CC-84	for external ROM, 12 MHz, ext. temperature – 40 to + 85 °C
SAB 80C517-N-T40/110	Q67120-C721	PL-CC-84	with factory mask-programmable ROM, 12 MHz, ext. temperature – 40 to + 110 °C
SAB 80C537-N-T40/110	Q67120-C571	PL-CC-84	for external ROM, 12 MHz, ext. temperature – 40 to + 110 °C
SAB 80C517-16-N	Q67120-C723	PL-CC-84	with mask-programmable ROM, 16 MHz
SAB 80C537-16-N	Q67120-C722	PL-CC-84	for external memory, 16 MHz
SAB 80C517-16-N-T40/85	Q67120-C724	PL-CC-84	with mask-programmable ROM, 16 MHz ext. temperature – 40 to + 85 °C
SAB 80C537-16-N-T40/85	Q67120-C725	PL-CC-84	for external memory, 16 MHz ext. temperature – 40 to + 85 °C
SAB 80C517-16-N-T40/110	Q67120-C726	PL-CC-84	with mask-programmable ROM, 16 MHz ext. temperature – 40 to + 110 °C
SAB 80C537-16-N-T40/110	Q67120-C727	PL-CC-84	for external memory, 16 MHz ext. temperature – 40 to + 110 °C
SAB 80C537-S-T40/110	Q67120-C717	P-QFP-100	for external memory, 12 MHz ext. temperature – 40 to + 110 °C

[1]) Other types of SAB 80C517/C80537 mounted in P-QFP-100 package: on request

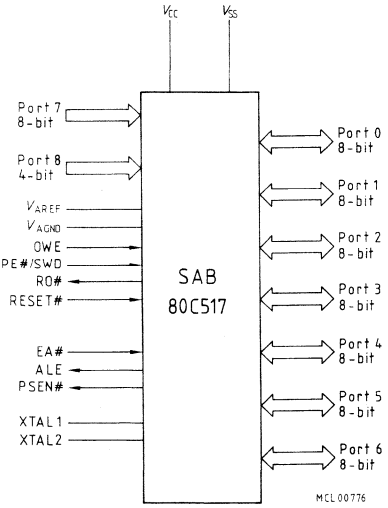
The SAB 80C517/80C537 is a high-end member of the Siemens SAB 8051 family of microcontrollers. It is designed in Siemens ACMOS technology and based on the SAB 8051 architecture. ACMOS is a technology which combines high-speed and density characteristics with low-power consumption or dissipation.

While maintaining all the SAB 80C515 features and operating characteristics the SAB 80C517 is expanded in its arithmetic capabilities, "fail-safe" characteristics, analog signal processing and timer capabilities. The SAB 80C537 is identical with the SAB 80C517 except that it lacks the on-chip program memory. The SAB 80C517/SAB 80C537 is supplied in a 84-pin plastic leaded chip carrier package (PL-CC-84).

Pin Configurations
(PL-CC-84)



Logic Symbol



Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	I/O	**Port 4** is a bidirectional I/O port with internal pullup resistors. Port 4 pins that have 1 s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. This port also serves alternate compare functions. The secondary functions are assigned to the pins of port 4 as follows: – CM0 (P4.0): Compare Channel 0 – CM1 (P4.1): Compare Channel 1 – CM2 (P4.2): Compare Channel 2 – CM3 (P4.3): Compare Channel 3 – CM4 (P4.4): Compare Channel 4 – CM5 (P4.5): Compare Channel 5 – CM6 (P4.6): Compare Channel 6 – CM7 (P4.7): Compare Channel 7
PE#/SWD	4	I	**Power saving mode enable#/ Start Watchdog Timer** A low level on this pin allows the software to enter the power down, idle and slow down mode. In case the low level is also seen during reset, the watchdog timer function is off on default. Use of the power saving modes is blocked, when this pin is held on high level. A high level during reset performs an automatic start of the watchdog timer immediately after reset. When left unconnected this pin is pulled high by a weak internal pullup resistor.
RESET#	10	I	**RESET#** A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80C517. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	11		**Reference voltage** for the A/D converter.
V_{AGND}	12		**Reference ground** for the A/D converter.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P7.7-P7.0	13-20	I	**Port 7** is an 8-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high/low voltages, and for the lower 8-bit of the multiplexed analog inputs of the A/D converter, simultaneously.
P3.0-P3.7	21-28	I/O	**Port 3** is a bidirectional I/O port with internal pull-up resistors. Port 3 pins that have 1 s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port 0 and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, als follows: – R × D (P3.0): receiver data input (asynchronous) or data input/output (synchronous) of serial interface – T × D (P3.1): transmitter data output (asynchronous) or clock output (synchronous) of serial interface 0 – INT0# (P3.2): interrupt 0 input#/timer 0 gate control – INT1# (P3.3): interrupt 1 input#/timer 1 gate control – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – WR# (P3.6): the write control signal latches the data byte from port 0 into the external data memory – RD# (P3.7): the read control signal enables the external data memory to port 0

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P1.7-P1.0	29-36	I/O	**Port 1** is a bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1 s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. It is used for the low order address byte during program verification. It also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows: – INT3#/CC0 (P1.0): interrupt 3 input#/ compare 0 output / capture 0 input – INT4/CC1 (P1.1): interrupt 4 input/ compare 1 output / capture 1 input – INT5/CC2 (P1.2): interrupt 5 input/ compare 2 output / capture 2 input – INT6/CC3 (P1.3): interrupt 6 input/ compare 3 output / capture 3 input – INT2#/CC4 (P1.4): interrupt 2 input#/ compare 4 output / capture 4 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input
XTAL2	39	–	**XTAL2** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL1	40	–	**XTAL1** Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P2.0-P2.7	41-48	I/O	**Port 2** is a bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1 s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup resistors when issuing 1 s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.
PSEN#	49	O	The **Program Store Enable#** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periodes except during external data memory accesses. Remains high during internal program execution.
ALE	50	O	The **Address Latch Enable** output is used for latching the address into external memory during normal operation. It is activated every six oscillator periodes except during an external data memory access.
EA#	51	I	**External Access Enable#** When held at high level, the SAB 80C517 executes instructions from the internal ROM when the PC is less than 8192. When held at low level, the SAB 80C517 fetches all instructions from external program memory. For the SAB 80C537 this pin must be tied low.

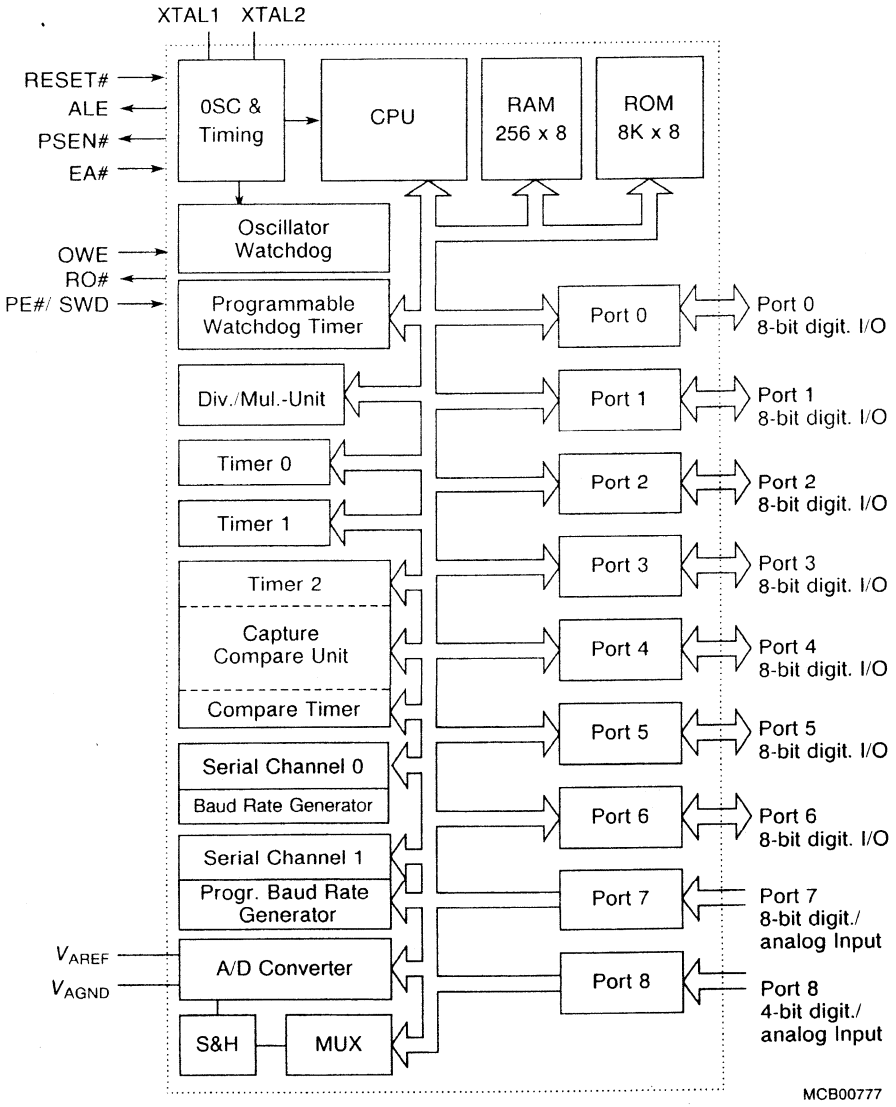
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P0.0-P0.7	52-59	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1 s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pullup resistors when issuing 1 s. Port 0 also outputs the code bytes during program verification in the SAB 80C517. External pullup resistors are required during program verification.
P5.7-P5.0	61-68	I/O	**Port 5** is a bidirectional I/O port with internal pullup resistors. Port 5 pins that have 1 s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. This port also serves the alternate function "Concurrent Compare". The secondary functions are assigned to the port 5 pins as follows: – CCM0 (P5.0): concurrent compare 0 – CCM1 (P5.1): concurrent compare 1 – CCM2 (P5.2): concurrent compare 2 – CCM3 (P5.3): concurrent compare 3 – CCM4 (P5.4): concurrent compare 4 – CCM5 (P5.5): concurrent compare 5 – CCM6 (P5.6): concurrent compare 6 – CCM7 (P5.7): concurrent compare 7
OWE	69	I	**Oscillator Watchdog Enable** A high level on this pin enables the oscillator watch-dog. When left unconnected this pin is pulled high by a weak internal pullup resistor. When held at low level the oscillator watchdog function is off.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
P6.0-P6.7	70-77	I/O	**Port 6** is a bidirectional I/O port with internal pull-up resistors. Port 6 pins that have 1 s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 6 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 6 also contains the external A/D converter control pin and the transmit and receive pins for serial channel 1. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 6, as follows: – ADST# (P6.0): external A/D converter start pin – R × D1 (P6.1): receiver data input of serial interface 1 – T × D1 (P6.2): transmitter data output of serial interface 1
P8.0-P8.3	78-81	I	**Port 8** is a 4-bit unidirectional input port. Port pins can be used for digital input, if voltage levels meet the specified input high/low voltages, and for the higher 4-bit of the multiplexed analog inputs of the A/D converter, simultaneously.
RO#	82	O	**Reset Output#** This pun outputs the internally synchronized reset request signal. This signal may be generated by an external hardware reset, a watchdog timer reset or an oscillator watchdog reset. The reset output is active low.
V_{SS}	37, 60, 83	–	**Circuit ground potential**
V_{CC}	38, 84	–	**Supply terminal** for all operating modes

Figure 1
Block Diagram



Functional Description

The SAB 80C517 is based on 8051 architecture. It is a fully compatible member of the Siemens SAB 8051/80C51 microcontroller family being a significantly enhanced SAB 80C515. The SAB 80C517 is therefore 100 % compatible with code written for the SAB 80C515.

CPU

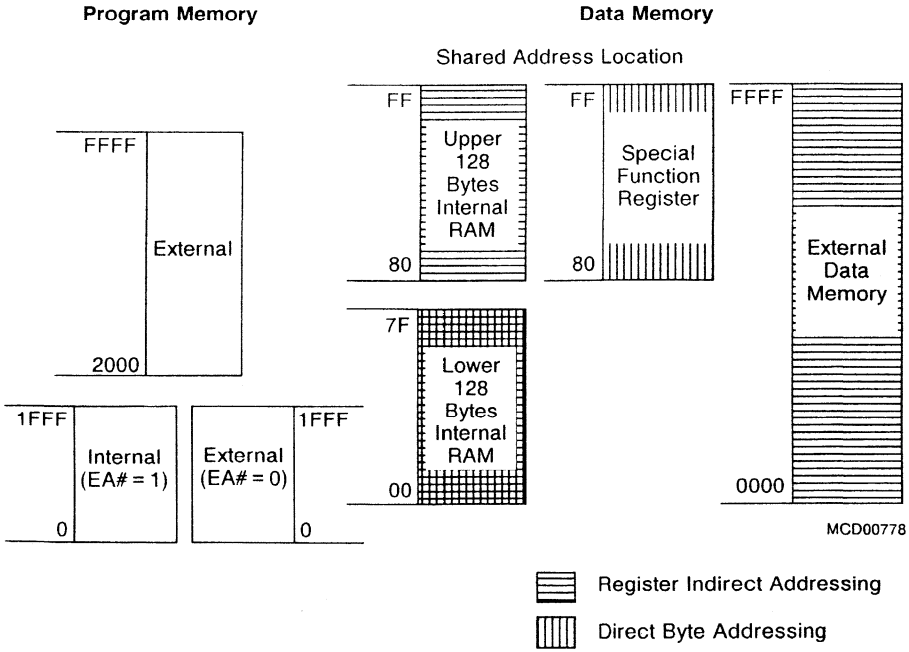
Having an 8-bit CPU with extensive facilities for bit-handling and binary BCD arithmetics the SAB 80C517 is optimized for control applications. With a 12 MHz crystal, 58 % of the instructions execute in 1 µs.

Being designed to close the performance gap to the 16-bit microcontroller world, the SAB 80C517's CPU is supported by a powerful 32-/16-bit arithmetic unit and a more flexible addressing of external memory by eight 16-bit datapointers.

Memory Organisation

According to the SAB 8051 architecture, the SAB 80C517 has separate address spaces for program and data memory. Figure 2 illustrates the mapping of address spaces.

Figure 2
Memory Mapping of the SAB 80C517



– Program Memory

The SAB 80C517 has 8 KByte of on-chip ROM, while the SAB 80C537 has no internal ROM. The program memory can externally be expanded up to 64 Kbyte. Pin EA# controls whether program fetches below address 2000H are done from internal or external memory.

– Data Memory

The data memory space consists of an internal and an external memory space.

– External Data Memory

Up to 64 KByte external data memory can be addressed by instructions that use 8-bit or 16-bit indirect addressing. For 8-bit addressing MOVX instructions utilizing registers R0 and R1 can be used. A 16-bit external memory addressing is supported by eight 16-bit datapointers.

Multiple Datapointers

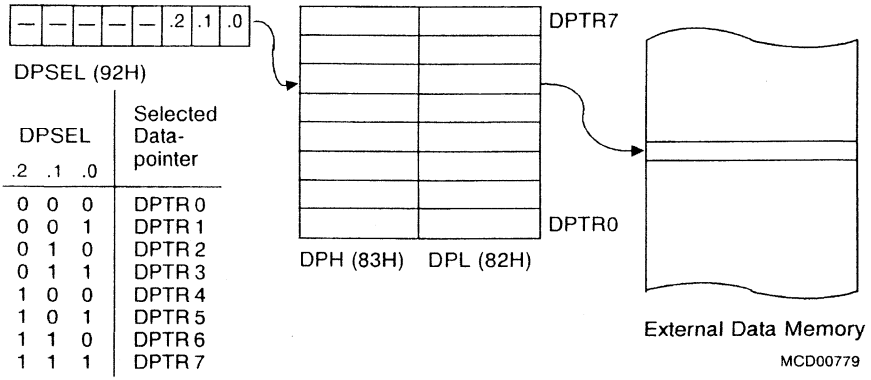
As a functional enhancement to standard 8051 controllers, the SAB 80C517 contains eight 16-bit datapointers. The instruction set uses just one of these datapointers at a time. The selection of the actual datapointers is done in special function register DPSEL (data pointer select, addr. 92H). Figure 3 illustrates the addressing mechanism.

Internal Data Memory

The internal data memory is divided into three physically distinct blocks:
– the lower 128 bytes of RAM including four banks of eight registers each
– the upper 128 byte of RAM
– the 128 byte special function register area.

A mapping of the internal data memory is also shown in figure 2. The overlapping address spaces are accessed by different addressing modes. The stack can be located anywhere in the internal data memory.

Figure 3
Addressing of External Data Memory



Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area. The 81 special function registers include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripherals. There are also 128 directly addressable bits within the SFR area. The special function registers are listed in table 1. In this table they are organized in groups which refer to the functional blocks of the SAB 80C517. Block names and symbols are listed in alphabetical order.

Table 1
Special Function Registers of the SAB 80C517

Block	Symbol	Name	Address	1)
CPU	ACC	Accumulator	0E0H	●
	B	B-Register	0F0H	●
	DPH	Data Pointer, High Byte	83H	
	DPL	Data Pointer, Low Byte	82H	
	DPSEL	Data Pointer Select Register	92H	
	PSW	Program Status Word Register	0D0H	●
	SP	Stack Pointer	81H	
A/D-Converter	ADCON0	A/D Converter Control Register 0	0D8H	●
	ADCON1	A/D Converter Control Register 1	0DCH	
	ADDAT	A/D Converter Data Register	0D9H	
	DAPR	D/A Converter Program Register	0DAH	
Interrupt System	IEN0	Interrupt Enable Register 0	0A8H	●
	CTCON 2)	Com. Timer Control Register	0E1H	
	IEN1	Interrupt Enable Register 1	0B8H	●
	IEN2	Interrupt Enable Register 2	9AH	
	IP0	Interrupt Priority Register 0	0A9H	
	IP1	Interrupt Priority Register 1	0B9H	
	IRCON	Interrupt Request Control Register	0C0H	●
	TCON 2)	Timer Control Register	88H	●
	T2CON 2)	Timer 2 Control Register	0C8H	●
MUL/DIV Unit	ARCON	Arithmetic Control Register	0EFH	
	MD0	Multiplication/Division Register 0	0E9H	
	MD1	Multiplication/Division Register 1	0EAH	
	MD2	Multiplication/Division Register 2	0EBH	
	MD3	Multiplication/Division Register 3	0ECH	
	MD4	Multiplication/Division Register 4	0EDH	
	MD5	Multiplication/Division Register 5	0EEH	

1) Bit-addressable special function registers are marked with a dot in this column.
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

Table 1(cont'd)
Special Function Registers of the SAB 80C517

Block	Symbol	Name	Address	1)
Compare/ Capture- Unit (CCU)	CCEN	Comp./Capture Enable Reg.	0C1H	
	CC4EN	Comp./Capture 4 Enable Reg.	0C9H	
	CCH1	Comp./Capture Reg. 1, High Byte	0C3H	
	CCH2	Comp./Capture Reg. 2, High Byte	0C5H	
	CCH3	Comp./Capture Reg. 3, High Byte	0C7H	
	CCH4	Comp./Capture Reg. 4, High Byte	0CFH	
	CCL1	Comp./Capture Reg. 1, Low Byte	0C2H	
	CCL2	Comp./Capture Reg. 2, Low Byte	0C4H	
	CCL3	Comp./Capture Reg. 3, Low Byte	0C6H	
	CCL4	Comp./Capture Reg. 4, Low Byte	0CEH	
	CMEN	Compare Enable Register	0F6H	
	CMH0	Compare Reg. 0, High Byte	0D3H	
	CMH1	Compare Reg. 1, High Byte	0D5H	
	CMH2	Compare Reg. 2, High Byte	0D7H	
	CMH3	Compare Reg. 3, High Byte	0E3H	
	CMH4	Compare Reg. 4, High Byte	0E5H	
	CMH5	Compare Reg. 5, High Byte	0E7H	
	CMH6	Compare Reg. 6, High Byte	0F3H	
	CMH7	Compare Reg. 7, High Byte	0F5H	
	CML0	Compare Register 0, Low Byte	0D2H	
	CML1	Compare Register 1, Low Byte	0D4H	
	CML2	Compare Register 2, Low Byte	0D6H	
	CML3	Compare Register 3, Low Byte	0E2H	
	CML4	Compare Register 4, Low Byte	0E4H	
	CML5	Compare Register 5, Low Byte	0E6H	
	CML6	Compare Register 6, Low Byte	0F2H	
	CML7	Compare Register 7, Low Byte	0F4H	
	CMSEL	Compare Input Select	0F7H	
	CRCH	Com./Rel./Capt. Reg. High Byte	0CBH	
	CRCL	Com./Rel./Capt. Reg. Low Byte	0CAH	
	CTCON	Com. Timer Control Reg.	0E1H	
	CTRELH	Com. Timer Rel. Reg., High Byte	0DFH	
	CTRELL	Com. Timer Rel. Reg., Low Byte	0DEH	
	TH2	Timer 2, High Byte	0CDH	
	TL2	Timer 2, Low Byte	0CCH	
	T2CON	Timer 2 Control Register	0C8H	●

1) Bit-addressable special function registers are marked with a dot in this column.

Table 1(cont'd)
Special Function Registers of the SAB 80C517

Block	Symbol	Name	Address	1)
Ports	P0	Port 0	80H	●
	P1	Port 1	90H	●
	P2	Port 2	0A0H	●
	P3	Port 3	0B0H	●
	P4	Port 4	0E8H	●
	P5	Port 5	0F8H	●
	P6	Port 6	0FAH	
	P7	Port 7, Analog/Digital Input	0DBH	
	P8	Port 8, Analog/Digital Input, 4-bit	0DDH	
Pow.Sav.M	PCON	Power Control Register	87H	
Serial Channels	ADCON0 2)	A/D Converter Control Reg.	0D8H	●
	PCON 2)	Power Control Register	87H	
	S0BUF	Serial Channel 0 Buffer Reg.	99H	
	S0CON	Serial Channel 0 Control Reg.	98H	●
	S1BUF	Serial Channel 1 Buffer Reg.	9CH	
	S1CON	Serial Channel 1 Control Reg.	9BH	
	S1REL	Serial Channel 1 Reload Reg.	9DH	
Timer 0/ Timer 1	TCON	Timer Control Register	88H	●
	TH0	Timer 0, High Byte	8CH	
	TH1	Timer 1, High Byte	8DH	
	TL0	Timer 0, Low Byte	8AH	
	TL1	Timer 1, Low Byte	8BH	
	TMOD	Timer Mode Register	89H	
Watchdog	IEN0 2)	Interrupt Enable Register 0	0A8H	●
	IEN1 2)	Interrupt Enable Register 1	0B8H	●
	IP0 2)	Interrupt Priority Register 0	0A9H	
	IP1 2)	Interrupt Priority Register 1	0B9H	
	WDTREL	Watchdog Timer Reload Reg.	86H	

1) Bit-addressable special function registers are marked with a dot in this column.
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

Table 2
Register Contents after Reset

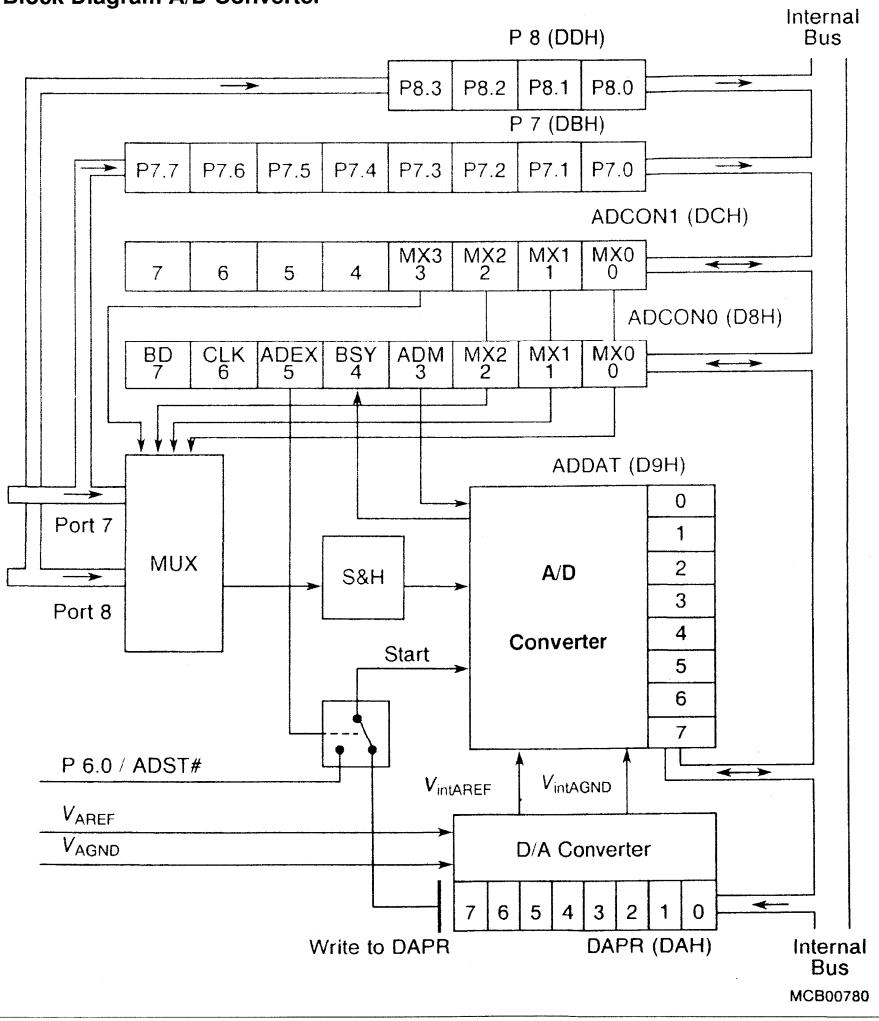
Register	Contents	Register	Contents
PC	000H	IEN0, IEN1	00H
ACC	00H	IEN2	XXXX 0XX0B
ADCON0	00H	IP0, IP1	00H, XX00 0000B
ADCON1	XXXX 0000B	IRCON	00H
ADDAT	00H	MD 0-5	XXH
ARCON	0XXXX XXXXB	P0-P6	0FFH
B	00H	PCON	00H
CCL1-4	00H	PSW	00H
CCH1-4	00H	S0BUF, S1BUF	0XXH
CCEN	00H	S0CON	00H
CC4EN	X000 0000B	S1CON	0X00 0000B
CMEN	00H	S1REL	00H
CMH0-7	00H	SP	07H
CML0-7	00H	TCON	00H
CMSEL	00H	TL0, TH0	00H
CRCL, CRCH	00H	TL1, TH1	00H
CTCON	XXXX 0000B	TL2, TH2	00H
CTRELL, CTRELH	00H	TMOD	00H
DAPR	00H	T2CON	00H
DPSEL	XXXXX000B	WDTREL	00H
DPTR0-7	0000H		

X means that the value is undeterminate

A/D Converter
The SAB 80C517 contains an 8-bit A/D Converter with 12 multiplexed input channels which uses the successive approximation method. It takes 7 machine cycles to sample an analog signal (during this sample time the input signal should be held constant); the total conversion time (including sample time) is 13 machine cycles (13 µs at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous; at the end of a conversion an interrupt can be generated.

A unique feature is the capability of internal reference voltage programming. The internal reference voltages $V_{intAREF}$ and $V_{intAGND}$ for the A/D converter are both programmable to one of 16 steps with respect to the external reference voltages. This feature permits a conversion with a smaller internal reference voltage range to gain a higher resolution. In addition, the internal reference voltages can easily be adapted by software to the desired analog input voltage range.

Figure 4
Block Diagram A/D Converter



Compare/Capture Unit (CCU)

The compare capture unit is a complex timer/register array for applications that require high speed I/O, pulse width modulation and more timer/counter capabilities. The CCU contains

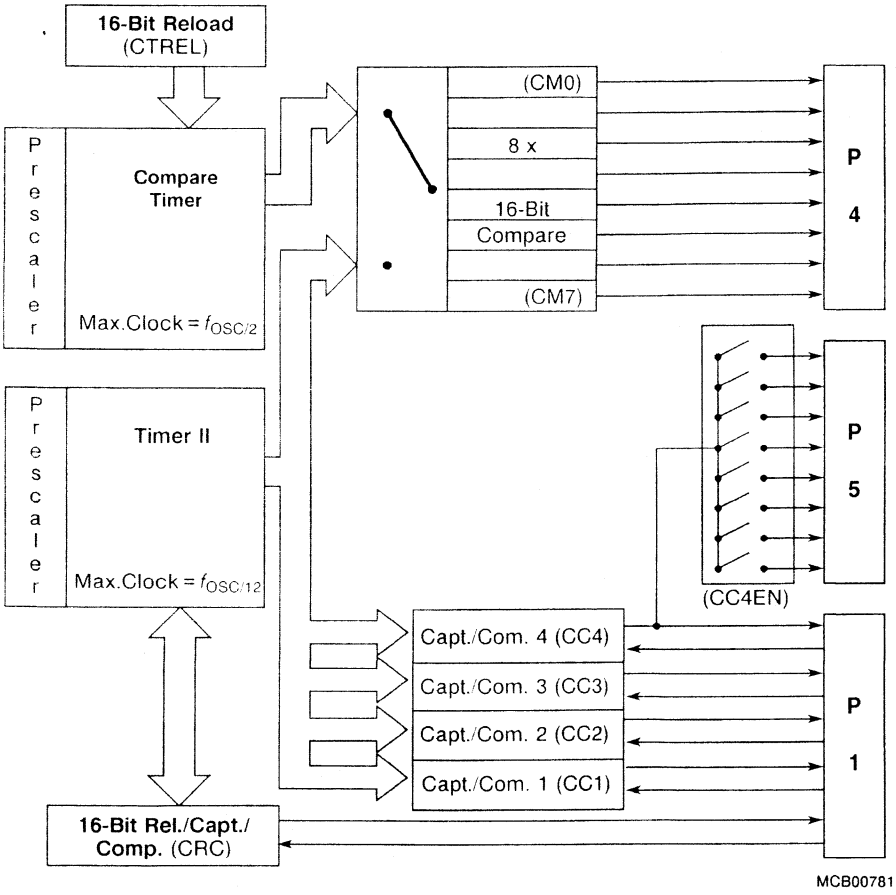
- one 16-bit timer/counter **(timer 2)** with 2-bit prescaler, reload capability and a max. clock frequency of $f_{osc}/12$ (1 MHz with a 12 MHz crystal).
- one 16-bit timer **(compare timer)** with 8-bit prescaler, reload capability and a max. clock frequency of $f_{osc}/2$ (6 MHz with a 12 MHz crystal).
- thirteen 16-bit compare registers.
- five of which can be used as 16-bit capture registers.
- up to 21 output lines controlled by the CCU.
- seven interrupts which can be generated by CCU-events.

Figure 5 shows a block diagram of the CCU. Eight compare registers (CM0 to CM7) can individually be assigned to either timer 2 or the compare timer. Diagrams of the two timers are shown in figures 6 and 7. The four compare/capture registers and the compare/reload/capture register are always connected to timer 2. Dependent on the register type and the assigned timer two compare modes can be selected. Table 3 illustrates possible combinations and the corresponding output lines.

Table 3
CCU Compare Configuration

Assigned Timer	Compare Register	Compare Output at	Possible Modes
Timer 2	CRCH/CRCL	P1.0/INT3#/CC0	Comp. mode 0, 1 + Reload
	CC1H/CC1L	P1.1/INT4/CC1	Comp. mode 0, 1
	CC2H/CC2L	P1.2/INT5/CC2	Comp. mode 0, 1
	CC3H/CC3L	P1.3/INT6/CC3	Comp. mode 0, 1
	CC4H/CC4L	P1.4/INT2#/CC4	Comp. mode 0, 1
	CC4H/CC4L	P5.0/CCM0	Comp. mode 1
	:	:	:
	CC4H/CC4L	P5.7/CCM7	Comp. mode 1
	CM0H/CM0L	P4.0/CM0	Comp. mode 1
	:	:	:
	CM7H/CM7L	P4.7/CM7	Comp. mode 1
Compare timer	CM0H/CM0L	P4.0/CM0	Comp. mode 0 (with add. latches)
	:	:	:
	CM7H/CM7L	P4.7/CM7	Comp. mode 0 (with add. latches)

Figure 5
Block Diagram of the Compare/Capture Unit



Compare

In the compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 register or the compare timer register. If the count value in the timer registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal changes from low to high. It goes back to low level when the timer overflows.

Mode 1: The transition of the output signal can be determined by software. A timer overflow signal doesn't affect the compare-output.

Compare registers CM0 to CM7 use additional compare latches when operated in mode 0. Figure 8 shows the function of these latches. The latches are implemented to prevent from loss of compare matches which may occur when loading of the compare values is not correlated with the timer count. The compare latches are automatically loaded from the compare registers at every timer overflow.

Capture

This feature permits saving of the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value of timer 2 registers into a dedicated capture register.

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

Reload of Timer 2

A 16-bit reload can be performed with the 16-bit CRC register, which is a concatenation of the 8-bit registers CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which also can request an interrupt.

Timer/Counters 0 and 1

These timer/counters are fully compatible with timer/counter 0 or 1 of the SAB 8051 and can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer; timer/counter 1 in this mode holds its count.

External inputs INT0# and INT1# can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

Figure 6
Block Diagram of Timer 2

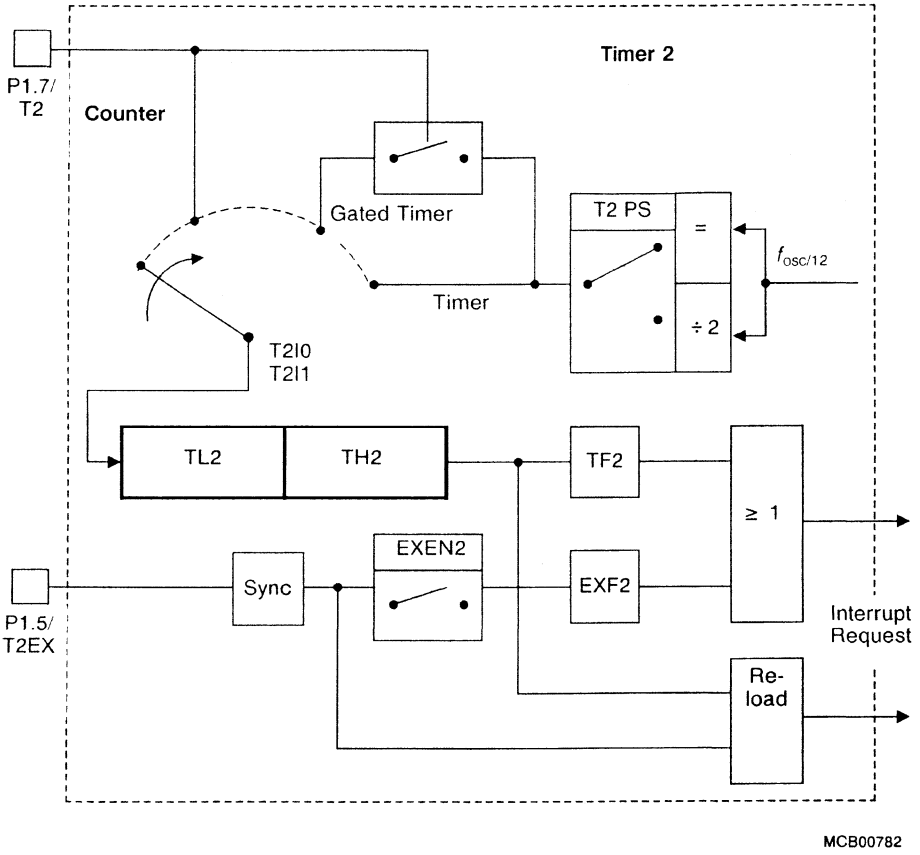


Figure 7
Block Diagram of the Compare Timer

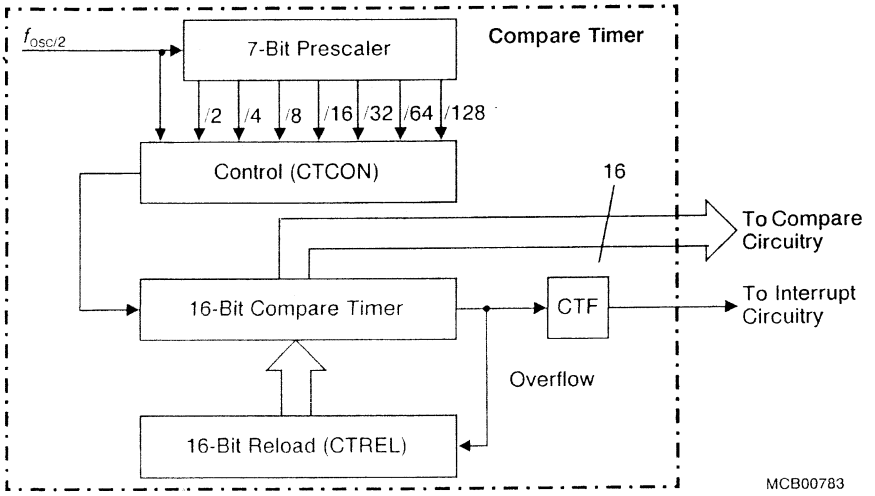
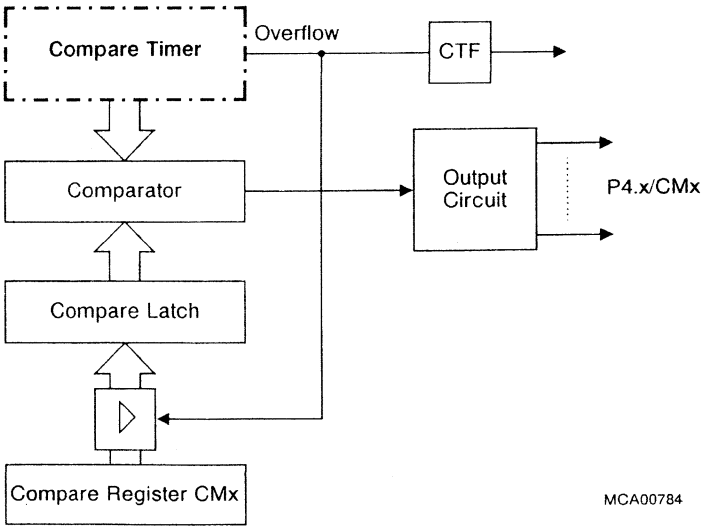


Figure 8
Compare-Mode 0 with Registers CM0 to CM7



Interrupt Structure

The SAB 80C517 has 14 interrupt vectors with the following vector addresses and request flags.

Table 4
Interrupt Sources and Vectors

Interrupt request flags	Interrupt vector address	Interrupt source
IE0	0003H	External interrupt 0
TF0	000BH	Timer 0 overflow
IE1	0013H	External interrupt 1
TF1	001BH	Timer 1 overflow
RI0/TI0	0023H	Serial channel 0
TF2/EXF2	002BH	Timer 2 overflow/ext. reload
IADC	0043H	A/D converter
IEX2	004BH	External interrupt 2
IEX3	0053H	External interrupt 3
IEX4	005BH	External interrupt 4
IEX5	0063H	External interrupt 5
IEX6	006BH	External interrupt 6
RI1/TI1	0083H	Serial channel 1
CTF	009BH	Compare timer overflow

Each interrupt vector can be individually enabled/disabled. The response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 2 to 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs or triples. Each pair or triple can be programmed individually to one of four priority levels by setting or clearing one bit in special function register IP0 and one in IP1. Figure 9 shows the interrupt request sources, the enabling and the priority level structure.

Figure 9
Interrupt Structure of the SAB 80C517

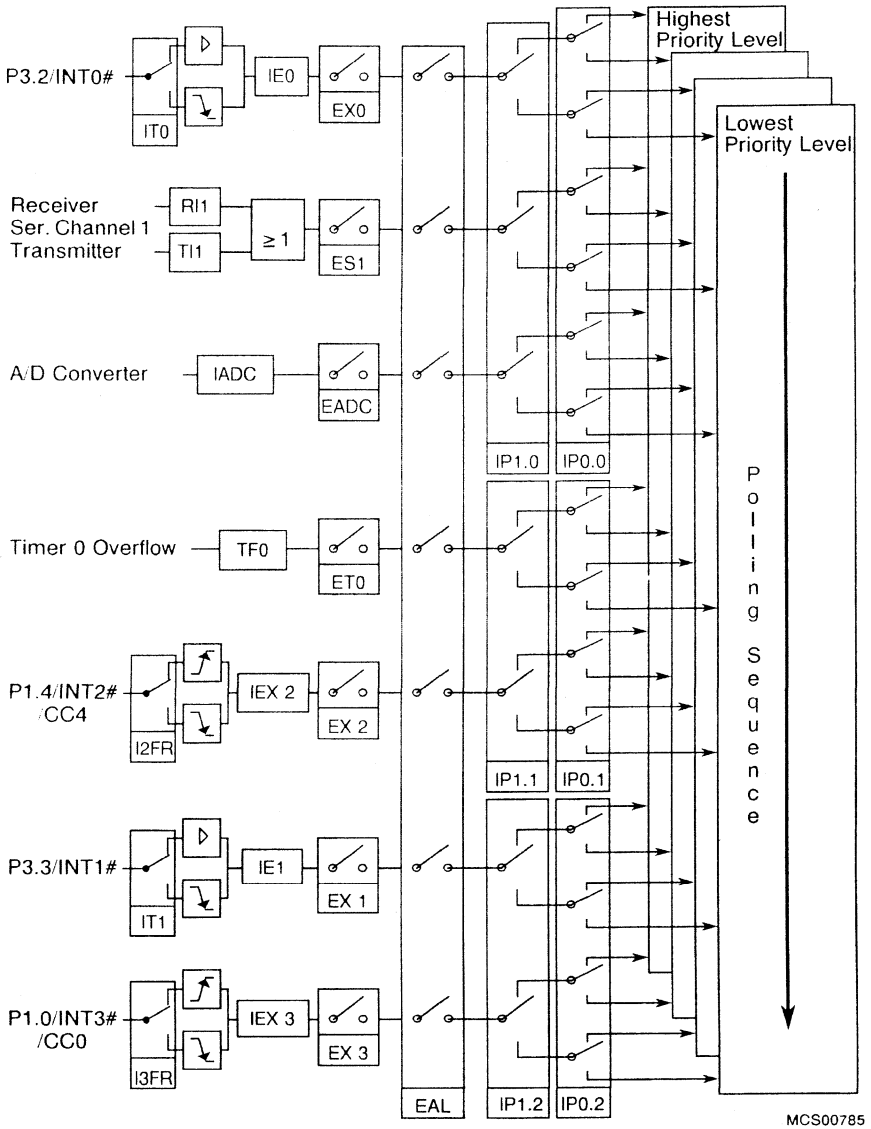
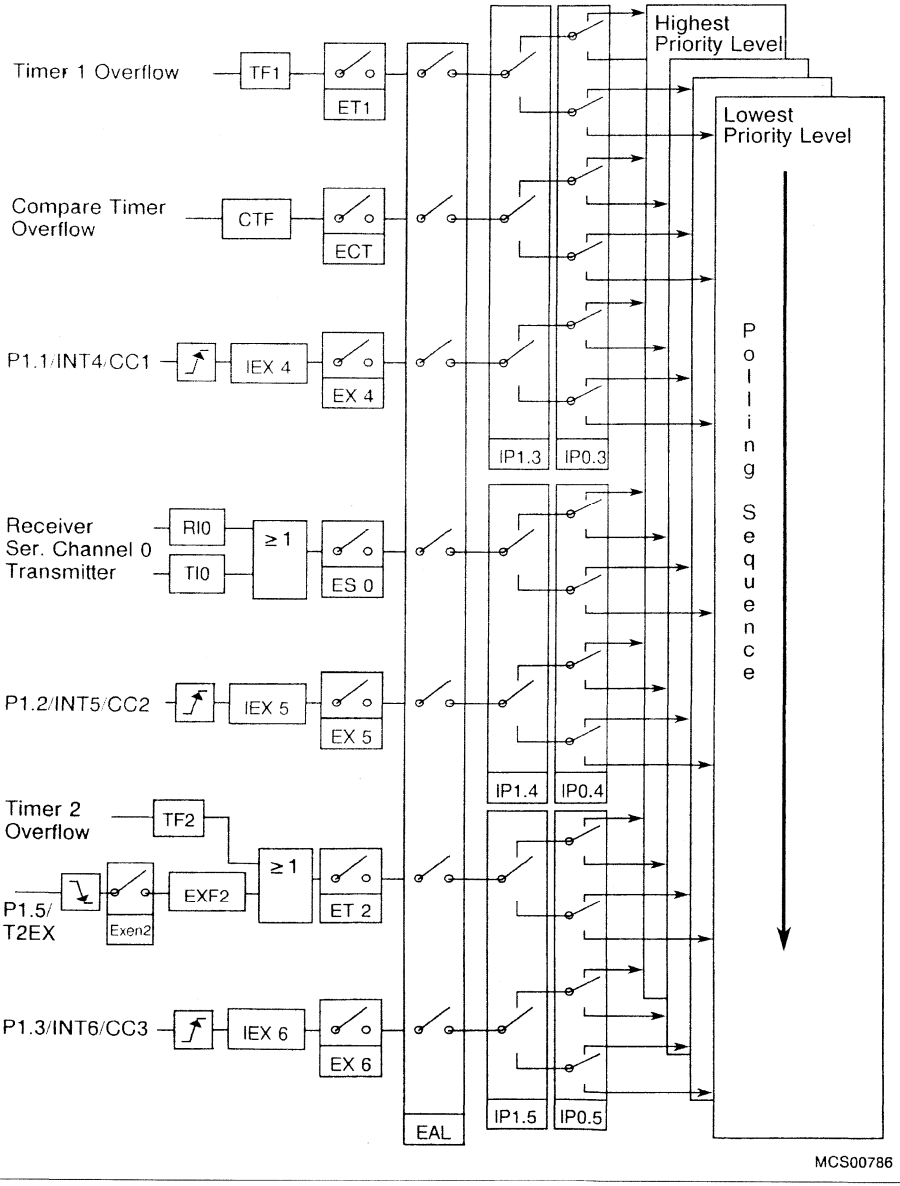


Figure 9
Interrupt Structure of the SAB 80C517



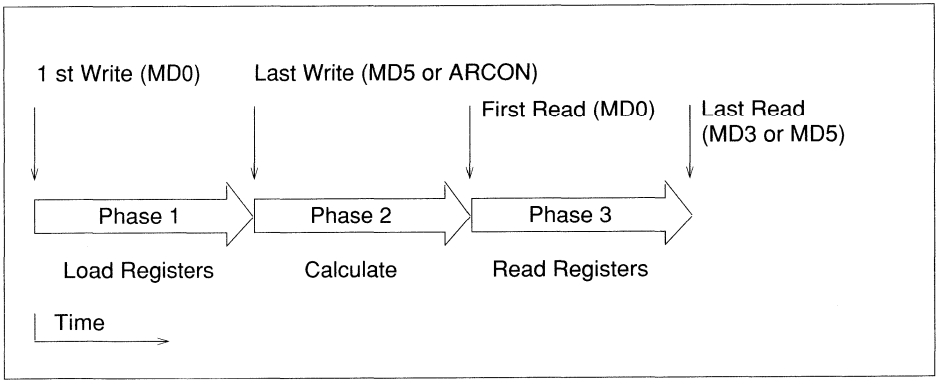
Multiplication/Division Unit

This on-chip arithmetic unit provides fast 32-bit division, 16-bit multiplication as well as shift and normalize features. All operations are integer operations.

Operation	Result	Remainder	Execution Time
32-bit/16-bit 16-bit/16-bit	32-bit 16-bit	16-bit 16-bit	$6t_{cy}$ [1] $4t_{cy}$
16-bit * 16-bit	32-bit	–	$4t_{cy}$
32-bit normalize	–	–	$6t_{cy}$ [2]
32-bit shift left/right	–	–	$6t_{cy}$ [2]

[1] $1t_{cy}$ = 1 µs @ 12 MHz oscillator frequency.
[2] The maximal shift speed is 6 shifts/cycle.

The MDU consists of six registers used for operands and results and one control register. Operation of the MDU can be divided in three phases:



To start an operation, register MD0 to MD5 (or ARCON) must be written to in a certain sequence according to table 5 or 6. The order the registers are accessed determines the type of the operation. A shift operation is started by a final write operation to register ARCON (see also the register description).

Table 5
Performing a MDU-Calculation

Operation	32-Bit/16-Bit	16-Bit/16-Bit	16-Bit * 16-Bit
First Write	MD0 D'endL MD1 D'end MD2 D'end MD3 D'endH MD4 D'orL	MD0 D'endL MD1 D'endH MD4 D'orL	MD0 M'andL MD4 M'orL MD1 M'andH
Last Write	MD5 D'orH	MD5 D'orH	MD5 M'orH
First Read	MD0 QuoL MD1 Quo MD2 Quo MD3 QuoH MD4 RemL	MD0 QuoL MD1 QuoH MD4 RemL	MD0 PrL MD1 Pr MD2 Pr
Last Read	MD5 RemH	MD5 RemH	MD3 PrH

Table 6
Shift Operation with the CCU

Operation	Normalize, Shift Left, Shift Right	
First Write	MD0	least significant byte
	MD1	
	MD2	
	MD3	most significant byte
Last Write	ARCON	start of conversion
First Read	MD0	least significant byte
	MD1	
	MD2	
Last Read	MD3	most significant byte

Abbreviations

D'end : Dividend, 1st operand of division
D'or : Divisor, 2nd operand of division
M'and : Multiplicand, 1st operand of multiplication
M'or : Multiplicator, 2nd operand of multiplication
Pr : Product, result of multiplication
Rem : Remainder
Quo : Quotient, result of division
...L : means, that this byte is the least significant of the 16-bit or 32-bit operand
...H : means, that this byte is the most significant of the 16-bit or 32-bit operand

I/O Ports

The SAB 80C517 has seven 8-bit I/O ports and two input ports (8-bit and 4-bit wide).

Port 0 is an open-drain bidirectional I/O port, while ports 1 to 6 are quasi-bidirectional I/O ports with internal pull-up resistors. That means, when configured as inputs, ports 1 to 6 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET. Port 1, 3, 4, 5 and ports 6 provide several alternate functions. Please see the "Pin Description" for details.

Port pins show the information written to the port latches, when used as general purpose port. When an alternate function is used, the port pin is controlled by the respective peripheral unit. Therefore the port latch must contain a "one" for that function to operate. The same applies when the port pins are used as inputs. Ports 1, 3, 4 and 5 are bit-addressable.

The SAB 80C517 has two dual-purpose input ports. The twelve port lines at port 7 and port 8 can be used as analog inputs for the A/D converter. If input voltages at P7 and P8 meet the specified digital input levels (V_{IL} and V_{IH}) the port can also be used as digital input port.

Power Saving Modes

The SAB 80C517 provides – due to Siemens ACMOS technology – three modes in which power consumption can be significantly reduced.

- The **Slow Down Mode**
  The controller keeps up the full operating functionality, but is driven with the eighth part of its normal operating frequency. Slowing down the frequency greatly reduces power consumption.
- The **Idle Mode**
  The CPU is gated off from the oscillator, but all peripherals are still supplied by the clock and able to work.
- The **Power Down Mode**
  Operation of the SAB 80C517 is stopped, the oscillator is turned off. This mode is used to save the contents of the internal RAM with a very low standby current.

All of these modes are entered by software. Special function register PCON (power control register, address is 87H) is used to select one of these modes.

Hardware Enable for Power Saving Modes

A dedicated Pin (PE#/SWD) of the SAB 80C517 allows to block the power saving modes. Since this pin is mostly used in noise-critical application it is combined with an automatic start of the Watchdog Timer (see there for further description).

PE#/SWD = V_{IH} (logic high level):

Using of the power saving modes is not possible. The instruction sequences used for entering of these modes will not affect the normal operation of the device.

PE#/SWD = V_{IL} (logic low level):

All power saving modes can be activated by software.
When left unconnected, Pin PE#/SWD is pulled to high level by a weak internal pullup. This is done to provide system protection on default.

The logic-level applied to pin PE#/SWD can be changed during program execution to allow or to block the use of the power saving modes without any effect on the on-chip watchdog circuitry.

Power Down Mode

The power down mode is entered by two consecutive instructions directly following each other. The first instruction has to set the flag PDE (power down enable) and must not set PDS (power down set). The following instruction has to set the start bit PDS. Bits PDE and PDS will automatically be cleared after having been set.

The instruction that sets bit PDS is the last instruction executed before going into power down mode. The only exit from power down mode is a hardware reset.

The status of all output lines of the controller can be looked up in table 7.

Table 7
Status of External Pins During Idle and Power Down

Outputs	Last instruction executed from internal code memory		Last instruction executed from external code memory	
	Idle	Power down	Idle	Power down
ALE	High	Low	High	Low
PSEN	High	Low	High	Low
Port 0	Data	Data	Float	Float
Port 1	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output
Port 2	Data	Data	Address	Data
Port 3	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output
Port 4	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output
Port 5	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output
Port 6	Data/alternate outputs	Data/last output	Data/alternate outputs	Data/last output

Idle Mode

During idle mode all peripherals of the SAB 80C517 are still supplied by the oscillator clock. Thus the user has to take care which peripheral should continue to run and which has to be stopped during Idle.

The procedure to enter the Idle mode is similar to entering the power down mode. The two bits IDLE and IDLS must be set by to consecutive instructions to minimize the chance of unintentional activating of the idle mode.

There are two ways to terminate the idle mode:

- The idle mode can be terminated by activating any enabled interrupt. This interrupt will be serviced and normally the instruction to be executed following the RETI instruction will be the one following the instruction that sets the bit IDLS.
- The other way to terminate the idle mode, is a hardware reset. Since the oscillator is still running, the hardware reset must be held active only for two machine cycles for a complete reset.

Normally the port pins hold the logical state they had at the time idle mode was activated. If some pins are programmed to serve their alternate functions they still continue to output during idle mode if the assigned function is on. The control signals ALE and PSEN# hold at logic high levels (see table 7).

Table 8
Baud Rate Generation

Function		Serial Interface 0		Serial Interface 1
8-bit synchronous channel	Mode	Mode 0		–
	Baud rate	1 MHz @ f_{osc} = 12 MHz		–
	Baud rate derived from	f_{osc}		–
8-bit UART	Mode	Mode 1		Mode B
	Baud rate *)	1 – 62.5 K	4800,9600	1.5 – 375 K
	Baud rate derived from	Timer 1	BD	8-bit baud rate generator
9-bit UART	Mode	Mode 2	Mode 3	Mode A
	Baud rate *)	187.5 K/ 375 K	1 – 62.5 K	1.5 – 375 K
	Baud rate derived from	$f_{osc}/2$	Timer 1	8-bit baud rate generator

*) Baud rate values are given for 12 MHz oscillator frequency.

Slow Down Mode

During slow down operation all signal frequencies that are derived from the oscillator clock, are divided by eight, also the clockout signal and the watchdog timer count.

The slow down mode is enabled by setting bit SD. The controller actually enters the slow down mode after a short synchronisation period (max. 2 machine cycles).

The slow down mode is disabled by clearing bit SD.

Serial Interfaces

The SAB 80C517 has two serial interfaces. Both interfaces are full duples and receive buffered. They are functionally identical with the serial interface of the SAB 8051 when working as asynchronous channels. Serial interface 0 additionally has a synchronous mode.

Serial Interface 0

Serial Interface 0 can operate in 4 modes:

Mode 0: Shift register mode:
Serial data enters and exits through R × D0. T × D0 outputs the shift clock 8 data bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 8-bit UART, variable baud rate:
10-bit are transmitted (through R × D0) or received (through R × D0): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On reception, the stop bit goes into RB80 in special function register S0CON. The baud rate is variable.

Mode 2: 9-bit UART, fixed baud rate:
11-bit are transmitted (through T × D0) or received (through R × D0): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). On transmission, the 9th data bit (TB80 in S0CON) can be assigned to the value of 0 or 1. For example, the parity bit (P in the PSW) could be moved into TB80 or a second stop bit by setting TB80 to 1. On reception the 9th data bit goes into RB80 in special function register S0CON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 9-bit UART, variable baud rate:
11-bit are transmitted (through T × D0) or received (through R × D0): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). In fact, mode 3 is the same as mode 2 in all respects except the baud rate. The baud rate in mode 3 is variable.

Variable Baud Rates for Serial Interface 0

Variable baud rates for modes 1 and 3 of serial interface 0 can be derived from either timer 1 or from the oscillator via a special prescaler ("BD").

Timer 1 may be operated in mode 1 (to generate slow baud rates) or mode 2. The dedicated baud rate generator "BD" provides the two standard baud rates 4800 or 9600 baud. Table 8 shows possible configurations and the according baud rates.

Serial Interface 1

Serial interface 1 can operate in two asynchronous modes:

Mode A: 9-bit UART, variable baud rate.
11 bits are transmitted (through T × D0) or received (through R × D0): a start bit (0), 8 data bits (LSB first), a programmable 9th, and a stop bit (1). On transmission, the 9th data bit (TB81 in S1CON) can be assigned to the value of 0 or 1. For example, the parity bit (P in the PSW) could be moved into TB81 or a second stop bit by setting TB81 to 1. On reception the 9th data bit goes into RB81 in special function register S1CON, while the stop bit is ignored.

Mode B: 8-bit UART, variable baud rate.
10 bits are transmitted (through T × D1) or received (through R × D1): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On reception, the stop bit goes into RB81 in special function register S1CON.

Variable Baud Rates for Serial Interface 1.

Variable baud rates for modes A and B of serial interface 1 can be derived from a dedicated baud rate generator.

The baud rate clock (baud rate = $\frac{\text{baud rate clock}}{16}$) is generated by a 8-bit free running timer with programmable reload register.

Watchdog Units

The SAB 80C517 offers two enhanced fail safe mechanisms, which allow an automatic recovery from hardware failure or software upset:

- programmable watchdog timer (WDT), variable from 512 µs up to about 1.1 s time out period @12 MHz. Upward compatible to SAB 80515 watchdog.
- oscillator watchdog (OWD), monitors the on-chip oscillator and forces the microcontroller to go into reset state, in case the on-chip oscillator fails.

Programmable Watchdog Timer

The WDT can be activated by hardware or software.

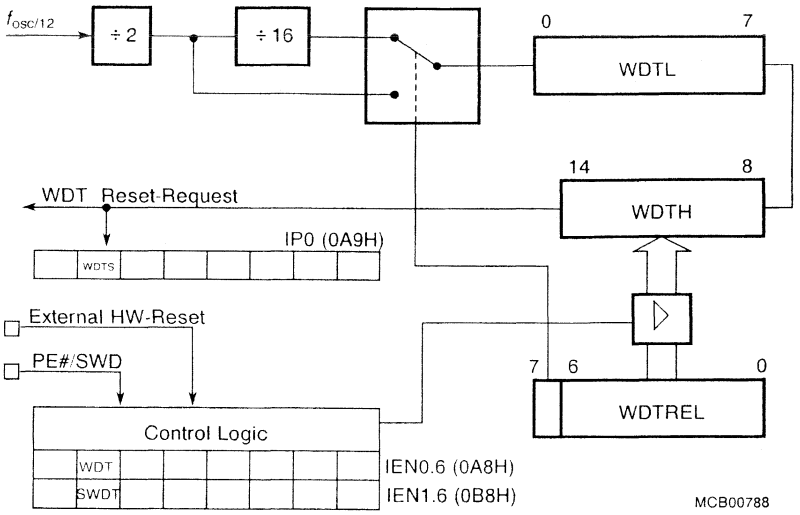
Hardware initialization is done when pin PE#/SWD (Pin 4) is held high during RESET. The SAB 80C517 then starts program execution with the WDT running. Pin PE#/SWD doesn't allow dynamic switching of the WDT.

Software initialization is done by setting bit SWDT. A refresh of the watchdog timer is done by setting bits WDT and SWDT consecutively.

A block diagram of the watchdog timer is shown in figure 10.

When a watchdog timer reset occurs, the watchdog timer keeps on running, but a status flag WDTS is set. This flag can also be manipulated by software.

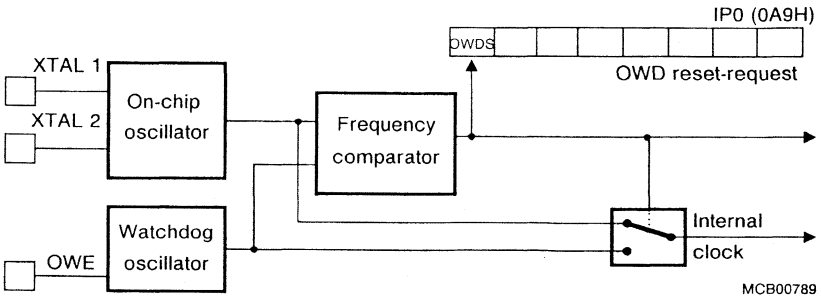
Figure 10
Block Diagram of the Programmable Watchdog Timer



Oscillator Watchdog

The oscillator watchdog monitors the on-chip quartz oscillator. A detected oscillator failure (f_{OSC} < appr. 300 kHz) causes a hardware reset. The reset state is held until the on-chip oscillator is working again. The oscillator watchdog feature is enabled by a high level at pin OWE (pin 69). An oscillator watchdog reset sets status flag OWDS which can be examined and modified by software. Figure 11 shows a block diagram of the oscillator watchdog.

Figure 11
Functional Block Diagram of the Oscillator Watchdog



Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct*)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct, A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2
MOV	direct,@R	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Notes on data addressing modes:

Rn – Working register R0 – R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is + 127/– 128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7

Hex code	Number of bytes	Mnemonic	Operands
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A, *#data*
25	2	ADD	A, *data addr*
26	1	ADD	A, @R0
27	1	ADD	A, @R1
28	1	ADD	A, R0
29	1	ADD	A, R1
2A	1	ADD	A, R2
2B	1	ADD	A, R3
2C	1	ADD	A, R4
2D	1	ADD	A, R5
2E	1	ADD	A, R6
2F	1	ADD	A, R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A, *#data*
35	2	ADDC	A, *data addr*
36	1	ADDC	A, @R0
37	1	ADDC	A, @R1
38	1	ADDC	A, R0
39	1	ADDC	A, R1
3A	1	ADDC	A, R2
3B	1	ADDC	A, R3
3C	1	ADDC	A, R4
3D	1	ADDC	A, R5
3E	1	ADDC	A, R6
3F	1	ADDC	A, R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*, A
43	3	ORL	*data addr, #data*
44	2	ORL	A, *#data*
45	2	ORL	A, *data addr*
46	1	ORL	A, @R0
47	1	ORL	A, @R1
48	1	ORL	A, R0
49	1	ORL	A, R1
4A	1	ORL	A, R2
4B	1	ORL	A, R3
4C	1	ORL	A, R4
4D	1	ORL	A, R5
4E	1	ORL	A, R6
4F	1	ORL	A, R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*, A
53	3	ANL	*data addr, #data*
54	2	ANL	A, *#data*
55	2	ANL	A, *data addr*
56	1	ANL	A, @R0
57	1	ANL	A, @R1
58	1	ANL	A, R0
59	1	ANL	A, R1
5A	1	ANL	A, R2
5B	1	ANL	A, R3
5C	1	ANL	A, R4
5D	1	ANL	A, R5
5E	1	ANL	A, R6
5F	1	ANL	A, R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*, A
63	3	XRL	*data addr, #data*
64	2	XRL	A, *#data*
65	2	XRL	A, *data addr*
66	1	XRL	A, @R0
67	1	XRL	A, @R1
68	1	XRL	A, R0
69	1	XRL	A, R1
6A	1	XRL	A, R2
6B	1	XRL	A, R3
6C	1	XRL	A, R4
6D	1	XRL	A, R5
6E	1	XRL	A, R6
6F	1	XRL	A, R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C, *bit addr*
73	1	JMP	@A + DPTR
74	2	MOV	A, *#data*
75	3	MOV	*data addr, #data*
76	2	MOV	@R0, *#data*
77	2	MOV	@R1, *#data*
78	2	MOV	R0, *#data*
79	2	MOV	R1, *#data*
7A	2	MOV	R2, *#data*
7B	2	MOV	R3, *#data*
7C	2	MOV	R4, *#data*
7D	2	MOV	R5, *#data*
7E	2	MOV	R6, *#data*
7F	2	MOV	R7, *#data*

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C, */bit addr*
83	1	MOVC	A, @A + PC
84	1	DIV	AB
85	3	MOV	*data addr, data addr*
86	2	MOV	*data addr,* @R0
87	2	MOV	*data addr,* @R1
88	2	MOV	*data addr,* R0
89	2	MOV	*data addr,* R1
8A	2	MOV	*data addr,* R2
8B	2	MOV	*data addr,* R3
8C	2	MOV	*data addr,* R4
8D	2	MOV	*data addr,* R5
8E	2	MOV	*data addr,* R6
8F	2	MOV	*data addr,* R7
90	3	MOV	DPTR, *#data*
91	2	ACALL	*code addr*
92	2	MOV	*/bit addr,* C
93	1	MOVC	A, @A + DPTR
94	2	SUBB	A, *#data*
95	2	SUBB	A, *data addr*
96	1	SUBB	A, @R0
97	1	SUBB	A, @R1
98	1	SUBB	A, R0
99	1	SUBB	A, R1
9A	1	SUBB	A, R2
9B	1	SUBB	A, R3
9C	1	SUBB	A, R4
9D	1	SUBB	A, R5
9E	1	SUBB	A, R6
9F	1	SUBB	A, R7

Hex code	Number of bytes	Mnemonic	Operands
A0	2	ORL	C, */bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C, */bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0, *data addr*
A7	2	MOV	@R1, *data addr*
A8	2	MOV	R0, *data addr*
A9	2	MOV	R1, *data addr*
AA	2	MOV	R2, *data addr*
AB	2	MOV	R3, *data addr*
AC	2	MOV	R4, *data addr*
AD	2	MOV	R5, *data addr*
AE	2	MOV	R6, *data addr*
AF	2	MOV	R7, *data addr*
B0	2	ANL	C, */bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A, *#data, code addr*
B5	3	CJNE	A, *data addr, code addr*
B6	3	CJNE	@R0,*#data, code addr*
B7	3	CJNE	@R1,*#data, code addr*
B8	3	CJNE	R0, *#data, code addr*
B9	3	CJNE	R1, *#data, code addr*
BA	3	CJNE	R2, *#data, code addr*
BB	3	CJNE	R3, *#data, code addr*
BC	3	CJNE	R4, *#data, code addr*
BD	3	CJNE	R5, *#data, code addr*
BE	3	CJNE	R6, *#data, code addr*
BF	3	CJNE	R7, *#data, code addr*

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A, *data addr*
C6	1	XCH	A, @R0
C7	1	XCH	A, @R1
C8	1	XCH	A, R0
C9	1	XCH	A, R1
CA	1	XCH	A, R2
CB	1	XCH	A, R3
CC	1	XCH	A, R4
CD	1	XCH	A, R5
CE	1	XCH	A, R6
CF	1	XCH	A, R7
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr, code addr*
D6	1	XCHD	A, @R0
D7	1	XCHD	A, @R1
D8	2	DJNZ	R0, *code addr*
D9	2	DJNZ	R1, *code addr*
DB	2	DJNZ	R3, *code addr*
DC	2	DJNZ	R4, *code addr*
DD	2	DJNZ	R5, *code addr*
DE	2	DJNZ	R6, *code addr*
DF	2	DJNZ	R7, *code addr*
E0	1	MOVX	A, @DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A, @R0
E3	1	MOVX	A, @R1
E4	1	CLR	A
E5	2	MOV	A, *data addr* *)
E6	1	MOV	A, @R0
E7	1	MOV	A, @R1
E8	1	MOV	A, R0
E9	1	MOV	A, R1
EA	1	MOV	A, R2
EB	1	MOV	A, R3
EC	1	MOV	A, R4
ED	1	MOV	A, R5
EE	1	MOV	A, R6
EF	1	MOV	A, R7
F0	1	MOVX	@DPTR, A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0, A
F3	1	MOVX	@R1, A
F4	1	CPL	A
F5	2	MOV	*data addr*, A
F6	1	MOV	@R0, A
F7	1	MOV	@R1, A
F8	1	MOV	R0, A
F9	1	MOV	R1, A
FA	1	MOV	R2, A
FB	1	MOV	R3, A
FC	1	MOV	R4, A
FD	1	MOV	R5, A
FE	1	MOV	R6, A
FF	1	MOV	R7, A

*) MOV A, ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	– 0 to 70 °C	(SAB 80C517/80C537)
	– 40 to + 85 °C	(SAB 80C517-/80C537-T40/85)
	– 40 to + 110 °C	(SAB 80C517-/80C537-T40/110)
Storage temperature	– 65 to150 °C	
Voltage on any pin with respect to ground (V_{SS})	– 0.5 to V_{CC} + 0.5 V	
Voltage on V_{CC} to V_{SS}	– 0.5 to + 6.5 V	
Power dissipation	2 W	

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for exetted periods may affect device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V; T_A = 0 to + 70 °C; for SAB 80C517/80C537
T_A = – 40 to + 85 °C; for SAB 80C517-/80C537-T40/85
T_A = – 40 to + 110 °C; for SAB 80C517-/80C537-T40/110

Symbol	Parameter	Limit values		Unit	Test Condition
		min.	max.		
V_{IL}	Input low voltage (except EA#)	– 0.5	0.2 V_{CC} – 0.1	V	–
V_{IL1}	Input low voltage (EA#)	– 0.5	0.2 V_{CC} – 0.3	V	–
V_{IH}	Input high voltage (except RESET# and XTAL2)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
V_{IH1}	Input high voltage to XTAL2)	0.7 V_{CC}	V_{CC} + 0.5	V	–
V_{IH2}	Input high voltage to RESET#	0.6 V_{CC}	V_{CC} + 0.5	V	–
V_{OL}	Output low voltage, (ports 1, 2, 3, 4, 5)	–	0.45	V	I_{OL} = 1.6 mA [1]
V_{OL1}	Output low voltage, (port 0, ALE, PSEN#, RO#)	–	0.45	V	I_{OL} = 3.2 mA [1]

Notes see page 276

DC Characteristics (cont'd)

Symbol	Parameter	Limit values		Unit	Test Condition
		min.	max.		
V_{OH}	Output high voltage (ports 1, 2, 3, 4, 5, 6)	2.4 0.9 V_{CC}	– –	V V	I_{OH} = – 80 µA [2] I_{OH} = – 10 µA [2]
V_{OH1}	Output high voltage (ports 0 in external bus mode, ALE, PSEN, RO#)	2.4 0.9 V_{CC}	– –	V V	I_{OH} = – 800 µA [2] I_{OH} = – 80 µA [2]
I_{IL}	Logic 0 input current (ports 1, 2, 3, 4, 5, 6)	–	– 50	µA	V_{IN} = 0.45 V
I_{IL2}	Input low current to RESET# for reset	–	– 100	µA	V_{IN} = 0.45 V
I_{IL3}	Input low current	–	– 10	µA	V_{IN} = 0.45 V
I_{TL}	Logical 1-to-0 transition current (ports 1, 2, 3, 4, 5, 6)	–	– 650	µA	V_{IN} = 2 V
I_{LI}	Input leakage current (port 0, EA#, ports 7, 8)	–	± 1	µA	0.45 < V_{IN} < V_{CC}
I_{LI2}	Input leakage current (OWEm PE#/SWD)	–	± 20	µA	0.45 < V_{IN} < V_{CC}
C_{IO}	Pin capacitance	–	10	pF	f_C = 1 MHz, T_A = 25°C
	Power-supply current:				
I_{CC}	– Active mode, 12 MHz [6]	–	40	mA	V_{CC} = 5 V [4]
	– Idle mode, 12 MHz [6]	–	15	mA	V_{CC} = 5 V [5]
	– Slow down mode, 12 MHz [6]	–	15	mA	V_{CC} = 5 V [5]
I_{CC}	– Active mode, 16 MHz [6]	–	52.3	mA	V_{CC} = 5 V [4]
	– Idle mode, 16 MHz [6]	–	19	mA	V_{CC} = 5 V [5]
	– Slow down mode, 16 MHz [6]	–	19	mA	V_{CC} = 5 V [5]
I_{PD}	– Power down mode	–	50	µA	V_{CC} = 2 ... 5.5 V

Notes see page 276

A/D Converter Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V; V_{AREF} = V_{CC} ± 5%; V_{AGND} = V_{SS} ± 0.2 V;
$V_{INTAREF} - V_{INTAGND} \geq 1$ V;
T_A = 0 to 70 °C for the SAB 80C517/80C537
T_A = – 40 to +85 °C for the SAB 80C517-80C537-T40/85
T_A = – 40 to +110 °C for the SAB 80C517-/80C537-T40/110

Symbol	Parameter	Limit values			Unit	Test Condition
		min.	typ.	max.		
V_{AINPUT}	Analog input voltage	V_{AGND} – 0.2	–	V_{AREF} + 0.2	V	9)
C_I	Analog input capacitance	–	25	60	pF	7)
t_L	Load time	–	–	2 t_{CY}	µs	7)
t_S	Sample time (incl. load time)	–	–	7 t_{CY}	µs	7)
t_C	Conversion time (incl. sample time)	–	–	13 t_{CY}	µs	7)
DNLE	Differential non-linearity	–	± 1/2	± 1	LSB	$V_{IntAREF}$ =
INLE	Integral non-linearity	–	± 1/2	± 1	LSB	V_{AREF} = V_{CC}
	Offset error		± 1/2	± 1	LSB	$V_{IntAGND}$ =
	Gain error		± 1/2	± 1	LSB	V_{AGND} = V_{SS}
TUE	Total unadjusted error		± 1	± 2	LSB	7)
$V_{IntREFERR}$	Internal reference error	–	–	TBD	mV	8)
I_{REF}	V_{AREF} supply current	–	–	5	mA	8)

Notes see page 276

Notes for pages 273 and 275

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1, 3, 4, and 5. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation.
In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN# to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.

3) Power down I_{PD} is measured with all output pins disconnected;
EA# = RESET# = V_{CC}; Port 0 = Port 7 = Port 8 = V_{CC}; XTAL1 = N.C.; XTAL2 = V_{SS};
PE#/SWD = OWE = V_{SS}.

4) I_{CC} (active mode) is measured with all output pins disconnected; XTAL2 driven with clock signal according to the figure below; XTAL1 = N.C.;
EA# = OWE = PE#/SWD = V_{CC}; Port 0 = Port 7 = Port 8 = V_{CC};
RESET# = V_{SS}. I_{CC} would be slightly higher if a crystal oscillator is used.

5) I_{CC} (idle mode,) is measured with all output pins disconnected and with all peripherals disabled; XTAL2 driven with clock signal according to the figure below; XTAL1 = N.C.;
RESET# = OWE = V_{CC}; Port 0 = Port 7 = Port 8 = V_{CC}; EA# = PE#/SWD = V_{SS}.

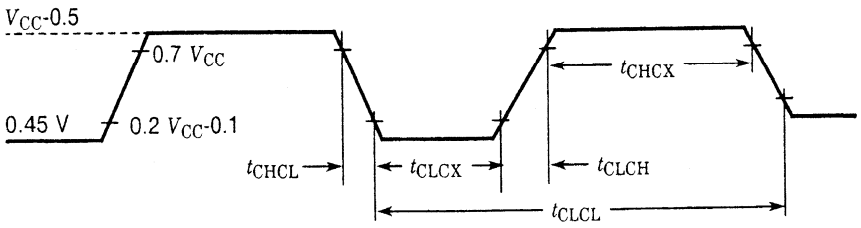
6) $I_{CC\,(max.)}$ at other frequencies is given by: active mode: $I_{CC\,max} = 3.1 * f_{OSC} + 3.0$
idle mode: $= 1.0 * f_{OSC} + 3.0$
Where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V (see also notes 4 and 5).

7) The output impedance of the analog source must be low enough to assure full loading of the sample capacitance (C_I) during load time (T_L). After charging of the internal capacitance (C_I) in the load time (T_L) the analog input must be held constant for the rest of the sample time (T_S).

8) The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

9) Exceeding the limit values at one or more input channels will cause additional current which is sinked sourced at these channels. This may also affect the accuracy of other channels which are operated

Clock Signal Waveform for I_{CC} Tests in Active and Idle Mode



AC Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V;

(C_L for port 0, ALE and PSEN# outputs = 100 pF; C_L for all outputs = 80 pF)

T_A = 0 to 70 °C for SAB 80C517/80C537
T_A = – 40 to + 85 °C for SAB 80C517/80C537-T40/85
T_A = – 40 to + 110 °C for SAB 80C517/80C537-T40/110

Symbol	Parameter	Limit values				Unit
		Clock 16 MHz		Variable clock $1/t_{CLCL}$ = 1 to 16 MHz		
		min.	max.	min.	max.	

Program Memory Characteristics

t_{LHLL}	ALE pulse width	85	–	$2t_{CLCL}$– 40	–	ns
t_{AVLL}	Address setup to ALE	33	–	t_{CLCL}– 30	–	ns
t_{LLAX}	Address hold after ALE	28	–	t_{CLCL}– 35	–	ns
t_{LLIV}	Address to valid instruction in	–	150	–	$4t_{CLCL}$– 100	ns
t_{LLPL}	ALE to PSEN#	38	–	t_{CLCL}– 25	–	ns
t_{PLPH}	PSEN# pulse width	153	–	$3t_{CLCL}$– 35	–	ns
t_{PLIV}	PSEN# to valid instruction in	–	88	–	$3t_{CLCL}$– 100	ns
t_{PXIX}	Input instruction hold after PSEN	0	–	0	–	ns
t_{PXIZ}	Input instruction float after PSEN# *)	–	43	–	t_{CLCL}– 20	ns
t_{PXAV}	Address valid after PSEN# *)	55	–	t_{CLCL}– 8	–	ns
t_{AVIV}	Address to valid instruction in	–	198	–	$5t_{CLCL}$– 115	ns
t_{AZPL}	Address float to PSEN#	0	–	0	–	ns

*) Interfacing the SAB 80C517 to devices with float times up to 55 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

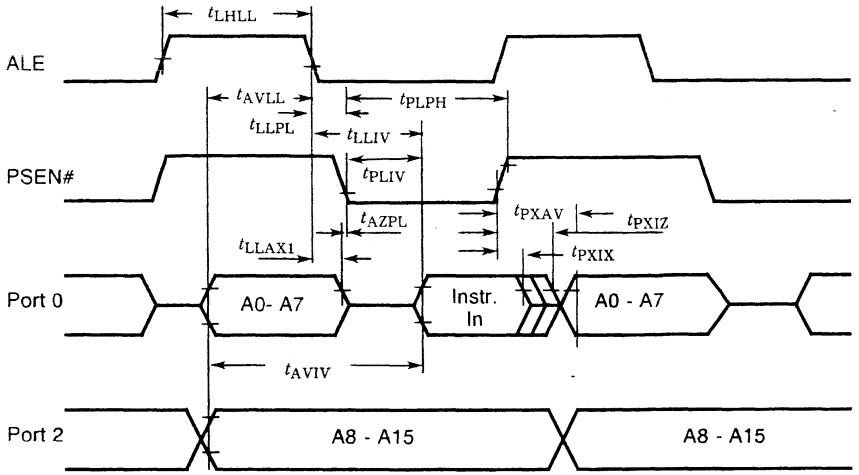
AC Characteristics (cont'd)

Symbol	Parameter	Limit values				Unit
		Clock 16 MHz		Variable clock $1/t_{CLCL}$ = 1 to 16 MHz		
		min.	max.	min.	max.	

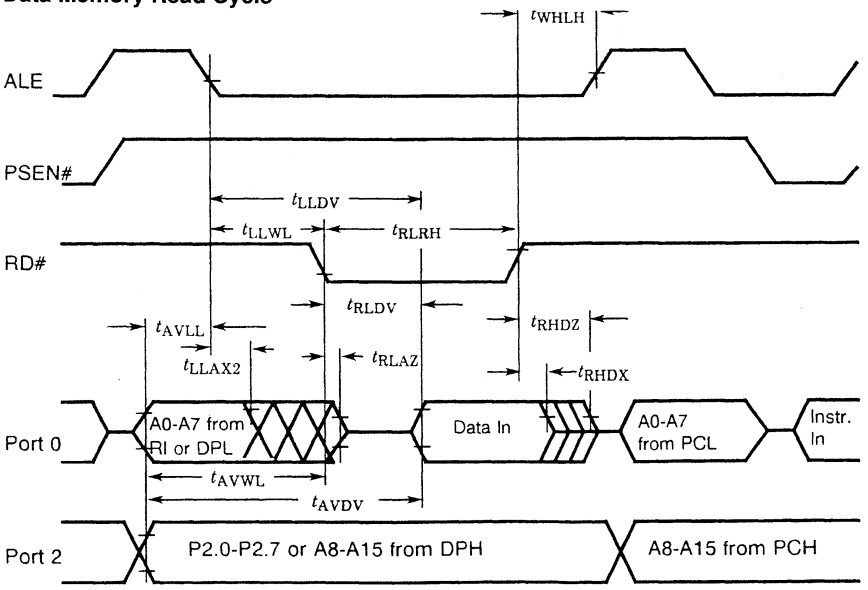
External Data Memory Characteristics

t_{RLRH}	RD# pulse width	275	–	$6t_{CLCL}$ – 100	–	ns
t_{WLWH}	WR# pulse width	275	–	$6t_{CLCL}$ – 100	–	ns
t_{LLAX2}	Address hold after ALE	90	–	$2t_{CLCL}$ – 35	–	ns
t_{RLDV}	RD# to valid data in	–	148	–	$5t_{CLCL}$ – 165	ns
t_{RHDX}	Data hold after RD#	0	–	0	–	ns
t_{RHDZ}	Data float after RD#	–	55	–	$2t_{CLCL}$ – 70	ns
t_{LLDV}	ALE to valid data in	–	350	–	$8t_{CLCL}$ – 150	ns
t_{AVDV}	Address to valid data in	–	398	–	$9t_{CLCL}$ – 165	ns
t_{LLWL}	ALE to WR# or RD#	138	238	$3t_{CLCL}$ – 50	$3t_{CLCL}$ + 50	ns
t_{WHLH}	WR# or RD# high to ALE high	23	103	t_{CLCL} – 40	t_{CLCL} + 40	ns
t_{AVWL}	Address valid to WR#	120	–	$4t_{CLCL}$ – 130	–	ns
t_{QVWX}	Data valid to WR# transition	13	–	t_{CLCL} – 50	–	ns
t_{QVWH}	Data setup before WR#	288	–	$7t_{CLCL}$ – 150	–	ns
t_{WHQX}	Data hold after WR#	13	–	t_{CLCL} – 50	–	ns
t_{RLAZ}	Address float after RD#	–	0	–	0	ns

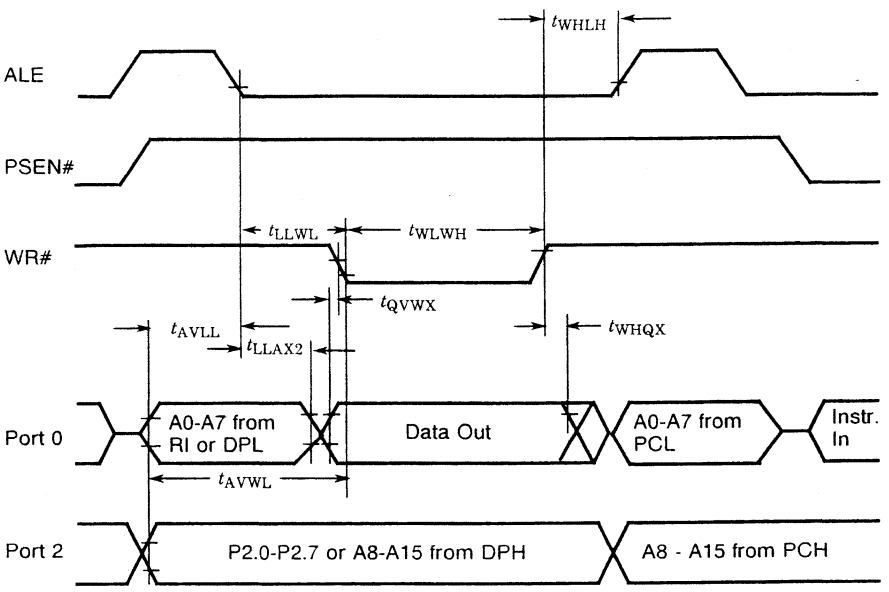
Program Memory Read Cycle



Data Memory Read Cycle



Data Memory Write Cycle



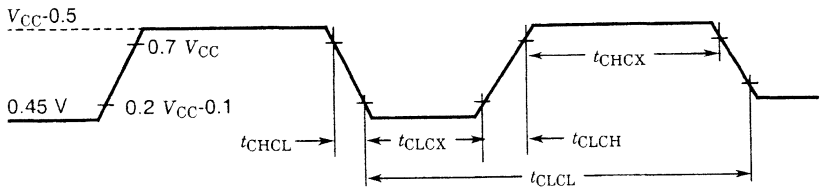
AC Characteristics (cont'd)

Symbol	Parameter	Limit Values		Unit
		Variable clock Frequ. = 1 to 16 MHz		
		min.	max.	

External Clock Drive

t_{CLCL}	Oscillator period	62.5	1000	ns
$1/t_{CLCL}$	Oscillator frequency	1	16	MHz
t_{CHCX}	High time	15	–	ns
t_{CLCX}	Low time	15	–	ns
t_{CLCH}	Rise time	–	15	ns
t_{CHCL}	Fall time	–	15	ns

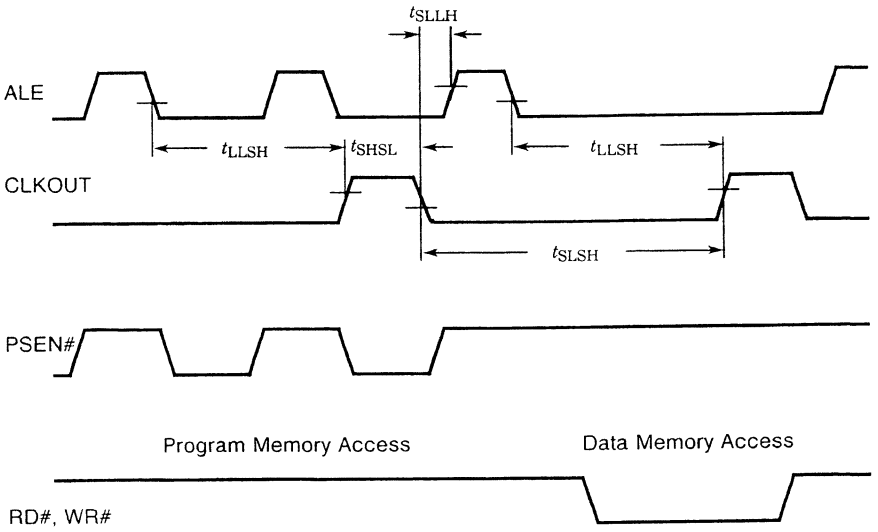
External Clock Cycle



AC Characteristics (cont'd)

Symbol	Parameter	Limit Values				Unit
		Clock 16 MHz		Variable clock $1/f_{CLCL}$ = 1 to 16 MHz		
		min.	max.	min.	max.	
System Clock Timing						
t_{LLSH}	ALE to CLKOUT	398	–	$7t_{CLCL} - 40$	–	ns
t_{SHSL}	CLKOUT high time	85	–	$2t_{CLCL} - 40$	–	ns
t_{SLSH}	CLKOUT low time	585	–	$10t_{CLCL} - 40$	–	ns
t_{SLLH}	CLKOUT low to ALE high	23	103	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns

System Clock Timing

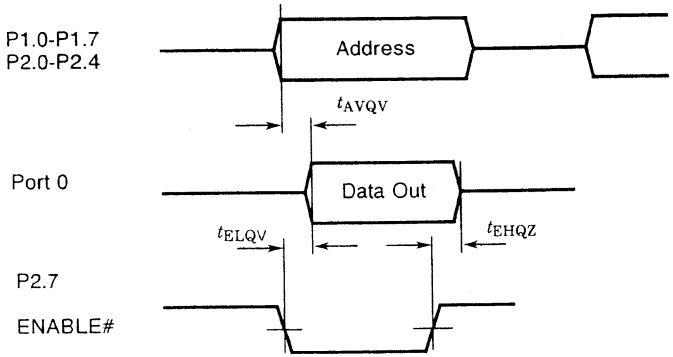


ROM Verification Characteristics

T_A = 25 °C ± 5 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	ENABLE to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after ENABLE	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification

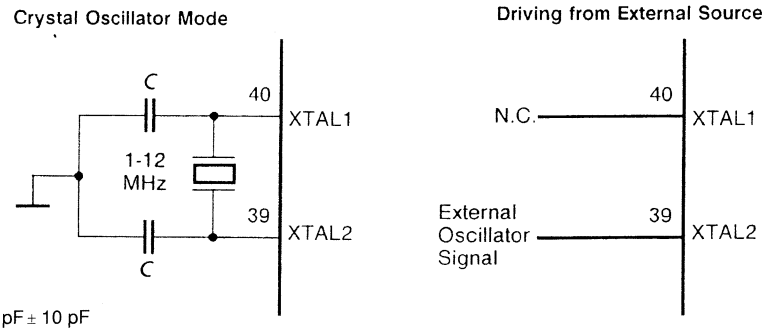


Address: P1.0–P1.7 = A0–A7
P2.0–P2.4 = A8–A12

Data: Port 0 = D0–D7

Inputs: P2.5 – P2.6, PSEN# = V_{SS}
ALE, EA # = V_{IH}
RESET# = V_{IL}

Recommended Oscilllator Circuits

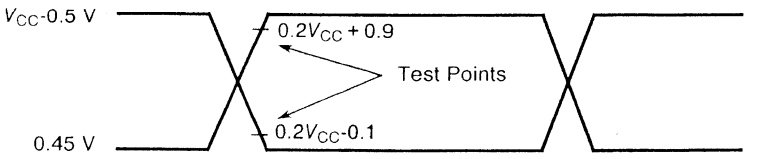


C 30 pF ± 10 pF
(incl. stray capacitance)

MCS00796

AC Testing

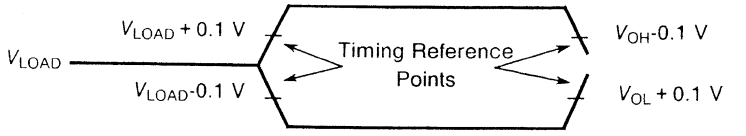
Input, Output Waveforms



MCA00697

AC Inputs during testing are driven at V_{CC} – 0.5 V for a logic 1 and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Float Waveforms



MCA00606

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm$ 20 mA.

SIEMENS

8-Bit Single Chip Microcontroller

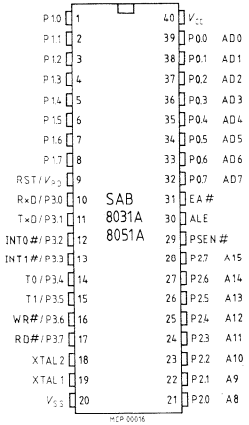
SAB 8051A/8031A

SAB 8051A/8051A-16 Microcontroller with factory maskprogrammable ROM
SAB 8031A/8031A-16 Microcontroller for external ROM

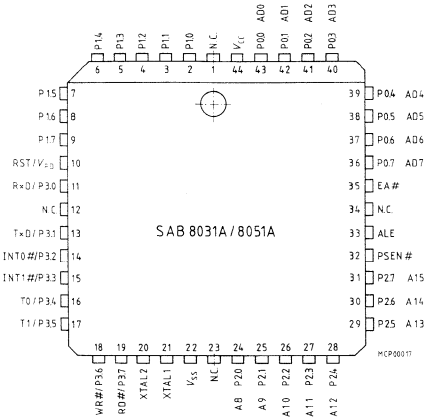
- SAB 8051A/8031A, 12 MHz operation
  SAB 8051A-16/8031A-16, 16 MHz operation
- 4K × 8 ROM
- 128 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- External memory expandable to 128 Kbyte
- High-performance full-duplex serial channel
- Compatible with SAB 8080/8085 peripherals
- Boolean processor
- 218 user bit-addressable locations
- Most instructions execute in: 1 µs (SAB 8051A/8031A) 750 ns
  (SAB 8051A-16/8031A-16)
- 4 µs (3 µs) multiply and divide
- P-DIP-40 and PL-CC-44 package

Pin Configuration

P-DIP-40



PL-CC-44

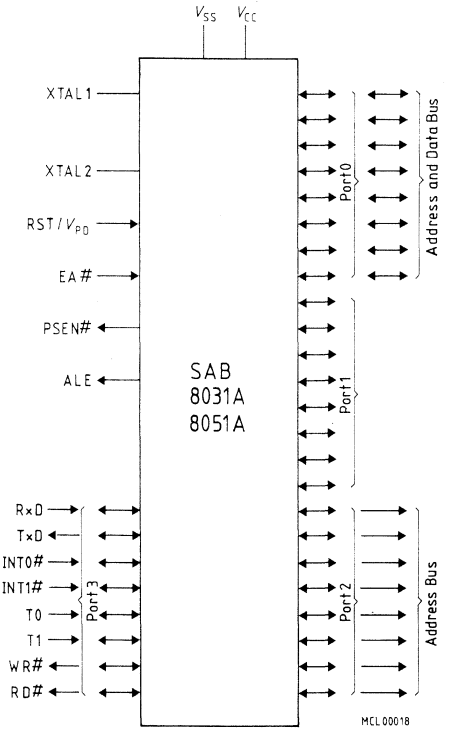


The SAB 8051A/8031A is a standalone, high-performance single-chip microcontroller fabricated in + 5 V advanced Siemens MYMOS (III) technology and supplied in a 40-pin plastic P-DIP or 44-pin plastic leaded chip carrier (PL-CC-44) package. It provides the hardware features, architectural enhancements and instructions that are necessary to make it a powerful and cost-effective controller for applications requiring up to 64 Kbytes of program memory and/or up to 64 Kbytes of data storage.

The SAB 8051A contains a non-volatile 4K × 8 read-only program memory; a volatile 128 × 8 read/write data memory; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full-duplex UART; and on-chip oscillator and clock circuits. The SAB 8031A is identical with the SAB 8051A, except that it lacks the program memory.

For systems that require extra capability, the SAB 8051A can be expanded using standard TTL-compatibel memories and the byte-oriented SAB 8080 and SAB 8085 peripherals.

Logic Symbol



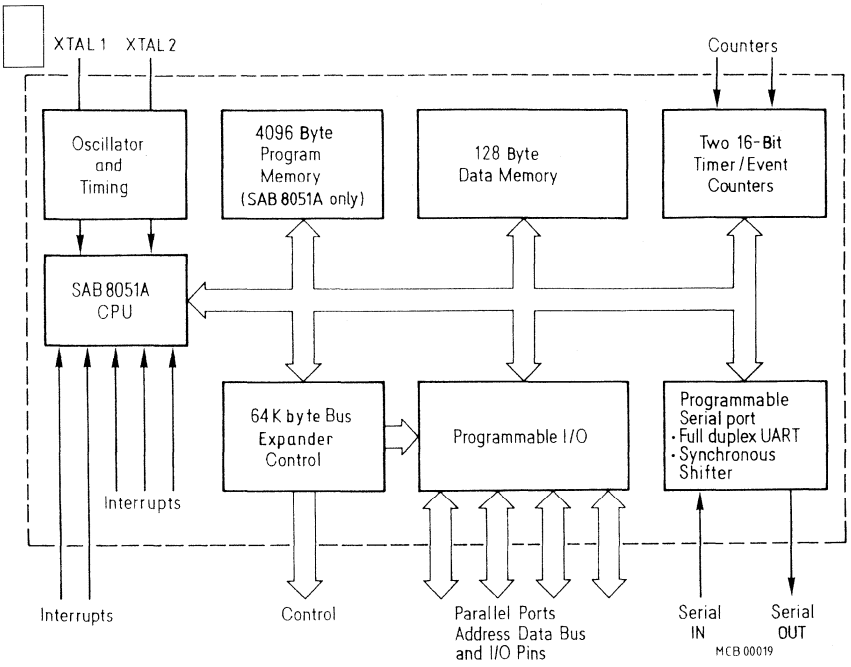
Pin Definitions and Functions

Symbol	Pin		Input (I) Output (O)	Function
	P-DIP-40	PL-CC-44		
P1.0-P1.7	1-8	2-9	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads.
RST/V_{PD}	9	10	I	A high level on this pin resets the SAB 8051A. A small internal pulldown resistor permits power-on reset using only a capacitor connected to V_{CC}. If V_{PD} is held within its spec while V_{CC} drops below spec, V_{PD} will provide standby power to the RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
P3.0-P3.7	10-17	11, 13-19	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of port 3, as follows: – R_XD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – T_XD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – INT0 (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – $\overline{T1}$ (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – $\overline{RD}$ (P3.7). The read control signal enables external data memory to port 0.
XTAL 1 XTAL 2	19 18	21 20	–	XTAL 1 input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to V_{SS} when external source is used on XTAL 2. XTAL 2 output from the oscillator's amplifier's. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0-P2.7	21-28	24-31	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.
$\overline{PSEN}$	29	32	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.

Pin Definitions and Functions (cont'd)

Symbol	Pin		Input (I) Output (O)	Function
	P-DIP-40	PL-CC-44		
ALE	30	33	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{EA}$	31	35	I	When held at a TTL high level, the SAB 8051A executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the SAB 8051A fetches all instructions from external program memory. For the SAB 8031A this pin must be tied low.
P0.0-P0.7	39-32	43-36	I/O	PORT 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
V_{CC}	40	44		+ 5 V power supply during operation and program verification.
V_{SS}	20	22		Ground (0 V)
NC	–	1, 12 23, 34	–	No connection

Block Diagram



Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations (cont'd)				
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct*)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct, A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer (cont'd)				
MOV	direct,@R	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0 – R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is + 127/– 128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr,code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr,code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,*#data*
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr,code addr*
31	2	ACALL	*code addr*
32	1	RETI	

Hex code	Number of bytes	Mnemonic	Operands
33	1	RLC	A
34	2	ADDC	A,*#data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr,#data*
44	2	ORL	A,*#data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr,#data*
54	2	ANL	A,*#data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr,#data*
64	2	XRL	A,*#data*
65	2	XRL	A,*data addr*

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
66	1	XRL	A,@R0
67	1	XRL	A,@R1
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr*,*data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*,R2
8B	2	MOV	*data addr*,R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data*,*code addr*
B5	3	CJNE	A,*data addr*,*code addr*
B6	3	CJNE	@R0,#*data*,*code addr*
B7	3	CJNE	@R1,#*data*,*code addr*
B8	3	CJNE	R0,#*data*,*code addr*
B9	3	CJNE	R1,#*data*,*code addr*
BA	3	CJNE	R2,#*data*,*code addr*
BB	3	CJNE	R3,#*data*,*code addr*
BC	3	CJNE	R4,#*data*,*code addr*
BD	3	CJNE	R5,#*data*,*code addr*
BE	3	CJNE	R6,#*data*,*code addr*
BF	3	CJNE	R7,#*data*,*code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr**)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr*,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	– 0 to + 70°C
Storage temperature	– 65 to + 150 °C
Voltage on any pin with respect to ground (V_{SS})	– 0.5 to + 7 V
Power dissipation	2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	Limit Values		Unit	Test Condition
		min.	max.		
V_{IL}	Input low voltage	– 0.5	0.8	V	–
V_{IH}	Input high voltage (except RST/VPD and XTAL 2)	2.0	V_{CC} + 0.5	V	–
V_{IH1}	Input high voltage to RST/VPD for reset, XTAL 2	2.5	V_{CC} + 0.5	V	XTAL1 to V_{SS}
V_{PD}	Power down voltage to RST/VPD	4.5	5.5	V	V_{CC} = 0 V
V_{OL}	Output low voltage Ports 1, 2, 3	–	0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output low voltage Port 0, ALE, $\overline{PSEN}$	–	0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output high voltage Ports 1, 2, 3	2.4	–	V	I_{OH} = – 80 µA
V_{OH1}	Output high voltage Port 0, ALE, $\overline{PSEN}$	2.4	–	V	I_{OH} = – 400 µA
I_{IL}	Logical 0 input current Ports 1, 2, 3	–	– 500	µA	V_{IL} = 0.45 V
I_{IL2}	Logical 0 input current XTAL 2	–	– 3.2	mA	XTAL 1 = V_{SS} V_{IL} = 0.45 V
I_{IH1}	Input high current to RST/V_{PD} for reset	–	500	µA	V_{IN} = V_{CC} – 1.5 V
I_{LI}	Input leakage current to port 0, $\overline{EA}$	–	± 10	µA	0 V < V_{IN} < V_{CC}
I_{CC}	Power supply current SAB 8031A/8051A SAB 8031A-16/8051A-16	– –	125 140	mA mA	All outputs disconnected
I_{PD}	Power down current	–	10	mA	V_{CC} = 0 V
C_{IO}	Capacitance of I/O buffer	–	10	pF	f_c = 1 MHz

AC Characteristics for SAB 8051A/8031A

T_A = 0 to + 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}-40$	–	ns
t_{AVLL}	Address setup to ALE	53	–	$t_{CLCL}-30$	–	ns
t_{LLAX1}	Address hold after ALE	48	–	$t_{CLCL}-35$	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	$4t_{CLCL}-100$	ns
t_{LLPL}	ALE to $\overline{PSEN}$	58	–	$t_{CLCL}-25$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	$3t_{CLCL}-35$	–	ns
t_{PLIV}	PSEN to valid instruction in	–	150	–	$3t_{CLCL}-100$	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float after $\overline{PSEN}$	–	63	–	$t_{CLCL}-20$	ns
t_{PXAV}*)	Address valid after $\overline{PSEN}$	75	–	$t_{CLCL}-8$	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	$5t_{CLCL}-115$	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

*) Interfacing the SAB 8051A to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

External Data Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	132	–	$2t_{CLCL}-35$	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	252	–	$5t_{CLCL}-165$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	$2t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	517	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	585	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	33	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

External Clock Drive XTAL2

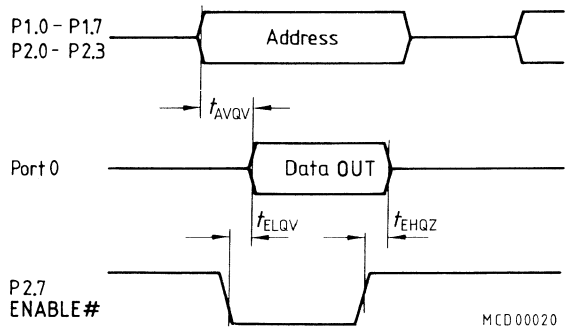
Symbol	Parameter	Limit Values		Unit
		Variable clock Freq = 1.2 MHz to 12 MHz		
		min.	max.	
t_{CLCL}	Oscillator period	83.3	833.3	ns
t_{CHCX}	High time	20	$t_{CLCL} - t_{CLCX}$	ns
t_{CLCX}	Low time	20	$t_{CLCL} - t_{CHCX}$	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

ROM Verification Characteristics for SAB 8051A

$T_A = 25\ °C \pm 5\ °C$; $V_{CC} = 5\ V \pm 10\%$; $V_{SS} = 0\ V$

Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	$\overline{\text{ENABLE}}$ to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after $\overline{\text{ENABLE}}$	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification



Address: P1.0–P1.7 = A0–A7
P2.0–P2.3 = A8–A11

Data: Port 0 = D0–D7

Inputs: P2.4 – P2.6, $\overline{\text{PSEN}}$ = V_{SS}
ALE, $\overline{\text{EA}}$ = V_{IH}
RST/V_{PD} = V_{IH1}

A/D Characteristics for SAB 8051A-16/8031A-16

T_A = 0 to + 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 16 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	85	–	$2t_{CLCL}$–40	–	ns
t_{AVLL}	Address setup to ALE	33	–	t_{CLCL}–30	–	ns
t_{LLAX1}	Address hold after ALE	28	–	t_{CLCL}–35	–	ns
t_{LLIV}	ALE to valid instruction in	–	150	–	$4t_{CLCL}$–100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	38	–	t_{CLCL}–25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	153	–	$3t_{CLCL}$–35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	88	–	$3t_{CLCL}$–100	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float after $\overline{PSEN}$	–	48	–	t_{CLCL}–15	ns
t_{PXAV}*)	Address valid after $\overline{PSEN}$	60	–	t_{CLCL}–3	–	ns
t_{AVIV}	Address to valid instruction in	–	223	–	$5t_{CLCL}$–90	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

*) Interfacing the SAB 8051A-16 to devices with float times up to 55 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

External Data Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	275	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	275	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	90	–	$2t_{CLCL}-35$	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	148	–	$5t_{CLCL}-165$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	55	–	$2t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	350	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	398	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	138	238	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	120	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	23	103	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	13	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	288	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	13	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

External Clock Drive XTAL2

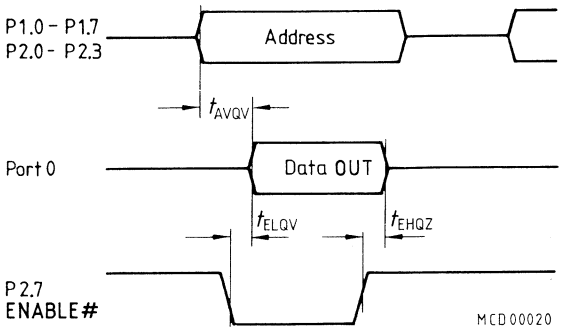
Symbol	Parameter	Limit Values		Unit
		Variable clock Freq = 1.2 MHz to 12 MHz		
		min.	max.	
t_{CLCL}	Oscillator period	62.5	833.3	ns
t_{CHCX}	High time	15	$t_{CLCL} - t_{CLCX}$	ns
t_{CLCX}	Low time	15	$t_{CLCL} - t_{CHCX}$	ns
t_{CLCH}	Rise time	–	15	ns
t_{CHCL}	Fall time	–	15	ns

ROM Verification Characteristics for SAB 8051A-16

T_A = 25 °C ± 5 °C; V_{CC} = 5V ± 10%; V_{SS} = 0 V

Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	$\overline{\text{ENABLE}}$ to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after $\overline{\text{ENABLE}}$	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification



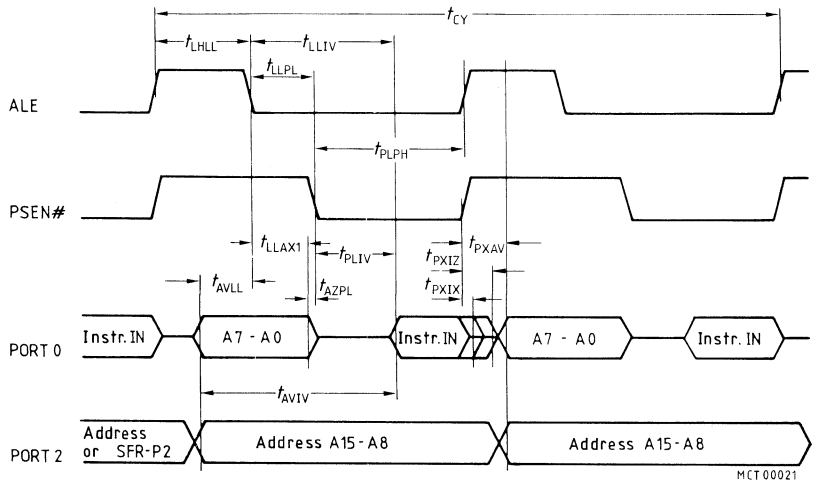
Address: P1.0–P1.7 = A0–A7
P2.0–P2.3 = A8–A11

Data: Port 0 = D0–D7

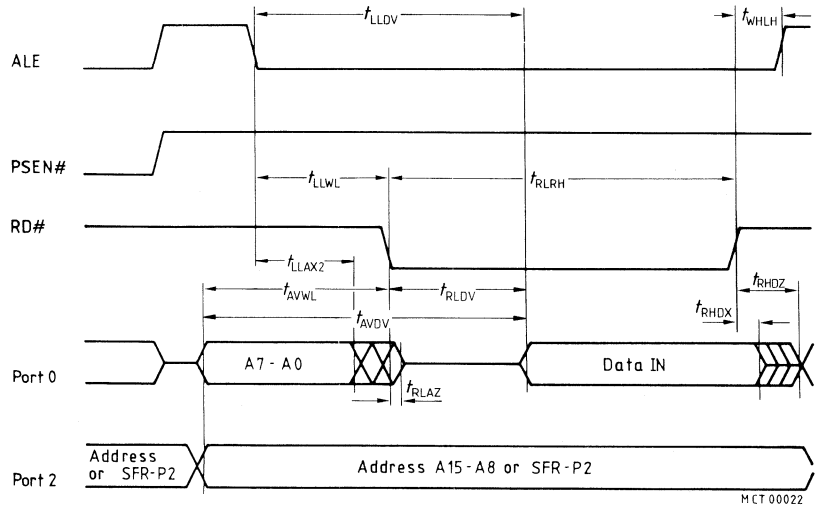
Inputs: P2.4 – P2.6, $\overline{\text{PSEN}}$ = V_{SS}
ALE, $\overline{\text{EA}}$ = V_{IH}
$\overline{\text{RST}}$/V_{PD} = V_{IH1}

Waveforms

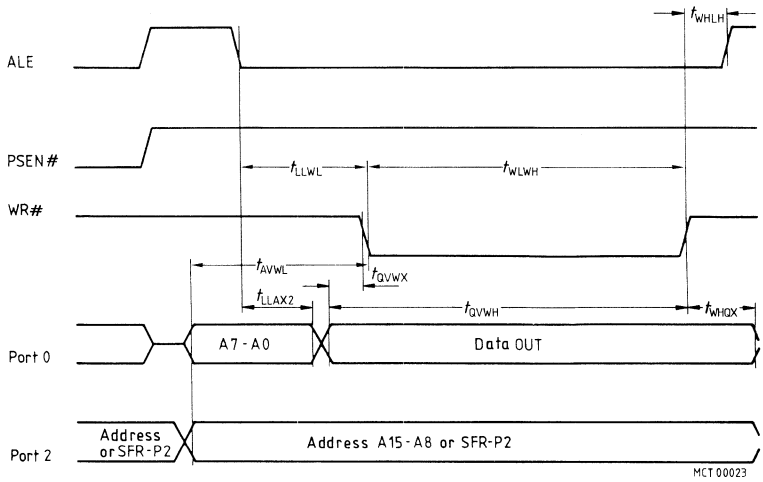
Program Memory Read Cycle



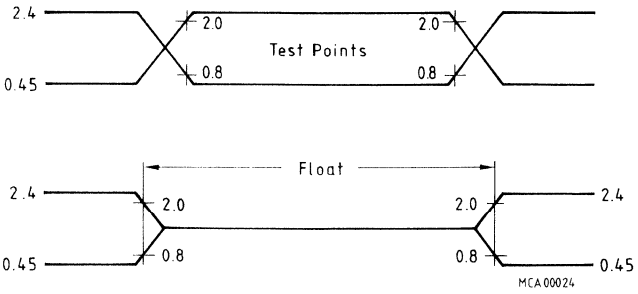
Data Memory Read Cycle



Data Memory Write Cycle

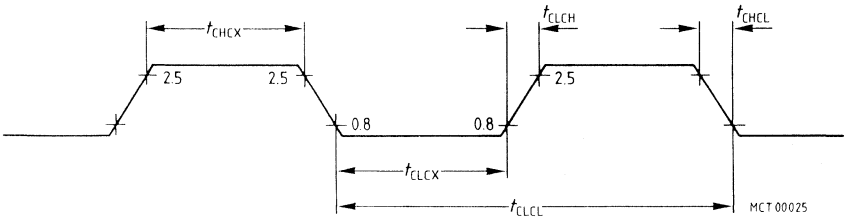


AC Testing Input, Output, Float Waveforms

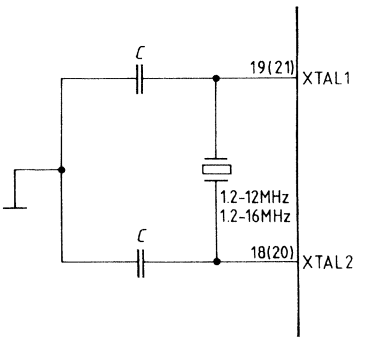


A.C. testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point where a P0 pin sinks 3.2 mA or sources 400 µA at voltage test levels.

External Clock Cycle

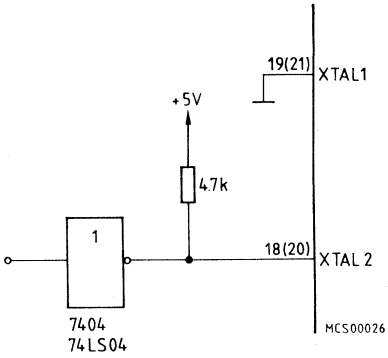


Recommended Oscillator Circuits



C = 30pF ± 10pF

Crystal Oscillator Mode



Driving from External Source

Pin number in (. . .) are for PL-CC-44 package

Ordering Information

Type	Ordering code	Description
		8-bit single-chip microcontroller,
SAB 8051A-P	Q 67120-C186	with mask-programmable ROM (P-DIP-40)
SAB 8031A-P	Q 67120-C183	for external memory (P-DIP-40)
SAB 8051A-16-P	Q 67120-C346	with mask-programmable ROM (P-DIP-40)
SAB 8031A-16-P	Q 67120-C347	for external memory (P-DIP-40)
SAB 8051A-N	Q 67120-C224	with mask-programmable ROM (PL-CC-44)
SAB 8031A-N	Q 67120-C271	for external memory (PL-CC-44)
SAB 8051A-16-N	Q 67120-C348	with mask-programmable ROM (PL-CC-44)
SAB 8031A-16-N	Q 67120-C349	for external memory (PL-CC-44)

SIEMENS

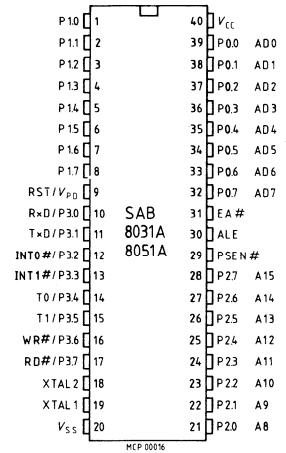
8-Bit Single-Chip Microcontroller — SAB 8051A/8031A Ext. Temp.

Extended Temperature Range: **– 40 to + 85 °C**
– 40 to +110 °C

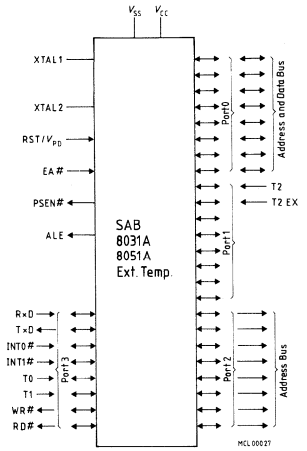
SAB 8051A-12-P-T40/85 **Mask-Program-** **SAB 8031A-12-P-T40/85** **External ROM**
SAB 8051A-10-P-T40/110 **mable ROM** **SAB 8031A-10-P-T40/110**

- Advanced version of the SAB 8031/8051 for extended temperature range
- SAB 8051A/8031A-12-T40/85: 12 MHz operation
- SAB 8051A/8031A-10-T40/110: 10 MHz operation
- 4K × 8 ROM
- 128 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- High-performance full-duplex serial channel
- Two 16-bit timer/event counters
- External memory expandable up to 128K
- Compatible with SAB 8080/8085 peripherals
- Boolean processor
- 218 user bit-addressable locations
- Most instructions execute in 1 µs
- 4 µs multiply and divide

Pin Configuration



Logic Symbol



The SAB 8051A/8031A for the two extended temperature ranges (industrial temperature range: – 40 to + 85 °C, automotive temperature range: – 40 to + 110 °C) is fully compatible with the standard SAB 8051A/8031A with respect to architecture, instruction set, and software portability.

The SAB 8051A/8031A is a stand-alone, high-performance single-chip microcontroller fabricated in + 5 V advanced N-channel, silicon gate Siemens MYMOS technology and packaged in a 40-pin DIP.

The SAB 8051A contains a non-volatile 4K × 8 read-only program memory; a volatile 128 × 8 read/write data memory; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and clock circuits. The SAB 8031A is identical with the SAB 8051A, except that it lacks the program memory.

For systems that require extra capability, the SAB 8051A can be expanded using standard TTL compatible memories and the byte-oriented SAB 8080 and SAB 8085 peripherals.

Ordering Information

Type	Ordering code	Description
		8-Bit Single-Chip-Microcontroller,
SAB 8051A-12-P-T40/85	Q 67120-C233	with mask-programmable ROM (Plastic)
SAB 8051A-10-P-T40/110	Q 67120-C231	with mask-programmable ROM (Plastic)
SAB 8031A-12-P-T40/85	Q 67120-C230	for external Memory (Plastic)
SAB 8031A-10-P-T40/110	Q 67120-C232	for external Memory (Plastic)

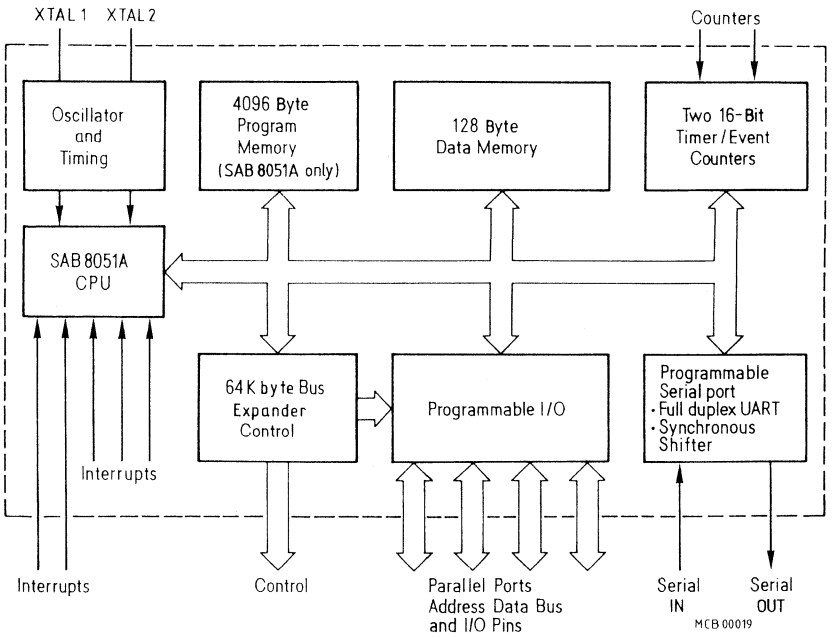
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Functions
P1.0-P1.7	1-8	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification.
RST/VPD	9	I	A high level on this pin resets the SAB 8051A. A small internal pulldown resistor permits power-on reset using only a capacitor connected to VCC. If VPD is held within its spec while VCC drops below spec, VPD will provide standby power to the RAM. When VPD is low, the RAM's current is drawn from VCC.
P3.0-P3.7	10-17	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of Port 3, as follows: – RxD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TxD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from Port 0 into the External Data Memory. – $\overline{RD}$ (P3.7). The read control signal enables External Data Memory to Port 0.
XTAL1 XTAL2	19 18		XTAL1 Input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to VSS when external source is used on XTAL2. XTAL2 Output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0-P2.7	21-28	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification.
$\overline{PSEN}$	29	O	The Program Store Enable output is a control signal that enables the external Program Memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	O	Provides Address Latch Enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{EA}$	31	I	When held at a high level, the SAB 8051A executes instructions from the internal ROM when the PC is less than 4096. When held at a low level, the SAB 8051A fetches all instructions from external Program Memory. For the SAB 8031A this pin must be tied low.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Functions
P0.0-P0.7	39-32	I/O	Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification.
VCC	40		+ 5 V power supply during operation and program verification.
VSS	20		Circuit ground potential

Block Diagram



Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A@Ri	AND indirect RAM to accumulator	1	1
ANL	A#data	AND immediate data to accumulator	2	1
ANL	direct, A	AND accumulator to direct byte	2	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations (cont'd)				
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct, A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct, A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate accumulator right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct*)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct, A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer (cont'd)				
MOV	direct,@R	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0 – R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is + 127/– 128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr,code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr,code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,*#data*
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr,code addr*
31	2	ACALL	*code addr*
32	1	RETI	

Hex code	Number of bytes	Mnemonic	Operands
33	1	RLC	A
34	2	ADDC	A,*#data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr,#data*
44	2	ORL	A,*#data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr,#data*
54	2	ANL	A,*#data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr,#data*
64	2	XRL	A,*#data*
65	2	XRL	A,*data addr*

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
66	1	XRL	A,@R0
67	1	XRL	A,@R1
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr*,*data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*,R2
8B	2	MOV	*data addr*,R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0

Hex code	Number of bytes	Mnemonic	Operands
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data*,*code addr*
B5	3	CJNE	A,*data addr*,*code addr*
B6	3	CJNE	@R0,#*data*,*code addr*
B7	3	CJNE	@R1,#*data*,*code addr*
B8	3	CJNE	R0,#*data*,*code addr*
B9	3	CJNE	R1,#*data*,*code addr*
BA	3	CJNE	R2,#*data*,*code addr*
BB	3	CJNE	R3,#*data*,*code addr*
BC	3	CJNE	R4,#*data*,*code addr*
BD	3	CJNE	R5,#*data*,*code addr*
BE	3	CJNE	R6,#*data*,*code addr*
BF	3	CJNE	R7,#*data*,*code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr**)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr*,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	– 40 to + 85 °C	for -T40/85
	– 40 to + 110 °C	for -T40/110
Storage temperature	– 65 to + 150 °C	
Voltage on any pin with respect to ground (V_{SS})	– 0.5 to + 7 V	
Power dissipation	2 W	

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V T_A = – 40 to + 85 °C for -T40/85
T_A = – 40 to + 110 °C for -T40/110

Symbol	Parameter	Limit Values		Unit	Test Condition
		min.	max.		
V_{IL}	Input low voltage	– 0.5	0.8	V	–
V_{IH}	Input high voltage except RST/VPD and XTAL 2	2.0	V_{CC} + 0.5	V	–
V_{IH1}	Input high voltage to RST/VPD for reset, XTAL 2	2.5	V_{CC} + 0.5	V	XTAL1 to V_{SS}
V_{PD}	Power down voltage to RST/VPD	4.5	5.5	V	V_{CC} = 0 V
V_{OL}	Output low voltage ports 1, 2, 3	–	0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output low voltage Port 0, ALE,/PSEN	–	0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output high voltage ports 1, 2, 3	2.4	–	V	I_{OH} = – 80 µA
V_{OH1}	Output high voltage Port 0, ALE,/PSEN	2.4	–	V	I_{OH} = – 400 µA
I_{IL}	Logical 0 input current ports 1, 2, 3	–	– 500	µA	V_{IL} = 0.45 V
I_{IL2}	Logical 0 input current XTAL 2	–	– 2.5	mA	XTAL 1 = V_{SS} V_{IL} = 0.45 V
I_{IH1}	Input high current to RST/VPD for reset	–	500	µA	V_{IN} = V_{CC} – 1.5 V
I_{LI}	Input leakage current to port 0,/EA	–	± 10	µA	0 < V_{IN} < V_{CC}
I_{CC}	Power supply current	–	150	mA	–
I_{PD}	Power down current	–	15	mA	
C_{IO}	Capacitance of I/O buffer	–	10	pF	f_c = 1 MHz

AC Characteristics for SAB T40/85

V_{CC} = 5 V ± 10%; V_{SS} = 0 V; T_A = − 40 to + 85 °C
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}-40$	–	ns
t_{AVLL}	Address setup to ALE	53	–	$t_{CLCL}-30$	–	ns
t_{LLAX1}	Address hold after ALE	48	–	$t_{CLCL}-35$	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	$4t_{CLCL}-100$	ns
t_{LLPL}	ALE to $\overline{PSEN}$	58	–	$t_{CLCL}-25$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	$3t_{CLCL}-35$	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	150	–	$3t_{CLCL}-100$	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float after $\overline{PSEN}$	–	63	–	$t_{CLCL}-20$	ns
t_{PXAV}*)	Address valid after $\overline{PSEN}$	75	–	$t_{CLCL}-8$	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	$5t_{CLCL}-115$	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

*) Interfacing the SAB 8051A to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

External Data Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	132	–	$2t_{CLCL}-35$	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	252	–	$5t_{CLCL}-165$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	$2t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	517	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	585	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	$3t_{CLCL}-50$	$3t_{CLCL}+50$	
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	33	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

AC Characteristics for T40/110

V_{CC} = 5 V ± 10%; V_{SS} = 0 V; T_A = – 40 to +110 °C
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		10 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 10 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	160	–	$2t_{CLCL}-40$	–	ns
t_{AVLL}	Address setup to ALE	70	–	$t_{CLCL}-30$	–	ns
t_{LLAX1}	Address hold after ALE	65	–	$t_{CLCL}-35$	–	ns
t_{LLIV}	ALE to valid instruction in	–	300	–	$4t_{CLCL}-100$	ns
t_{LLPL}	ALE to $\overline{PSEN}$	75	–	$t_{CLCL}-25$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	265	–	$3t_{CLCL}-35$	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	200	–	$3t_{CLCL}-100$	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float after $\overline{PSEN}$	–	80	–	$t_{CLCL}-20$	ns
t_{PXAV}*)	Address valid after $\overline{PSEN}$	92	–	$t_{CLCL}-8$	–	ns
t_{AVIV}	Address to valid instruction in	–	385	–	$5t_{CLCL}-115$	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

*) Interfacing the SAB 8051A to devices with float times up to 92 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

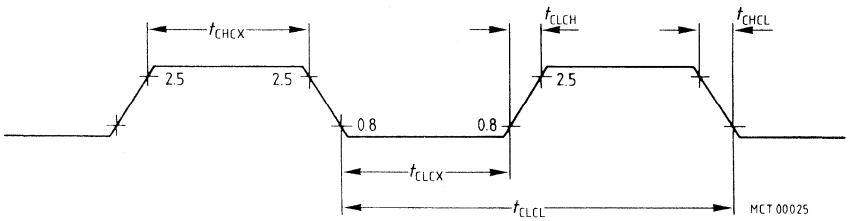
External Data Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		10 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 10 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	500	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	500	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	165	–	$2t_{CLCL}-35$	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	335	–	$5t_{CLCL}-165$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	130	–	$2t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	650	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	735	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	250	350	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	270	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	60	140	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	50	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	550	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	50	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

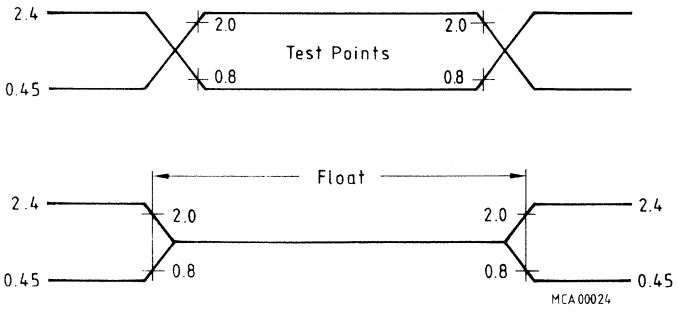
External Clock Drive XTAL2

Symbol	Parameter	Limit Values		Unit
		Variable clock Freq = 1.2 MHz to 12 MHz (T40/ 85) Freq = 1.2 MHz to 10 MHz (T40/110)		
		min.	max.	
t_{CLCL}	Oscillator period T40/85 T40/110	83.3 100	833.3	ns
t_{CHCX}	High time	20	$t_{CLCL} - t_{CLCX}$	ns
t_{CLCX}	Low time	20	$t_{CLCL} - t_{CHCX}$	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

External Clock Cycle



AC Testing Input, Output, Float Waveforms



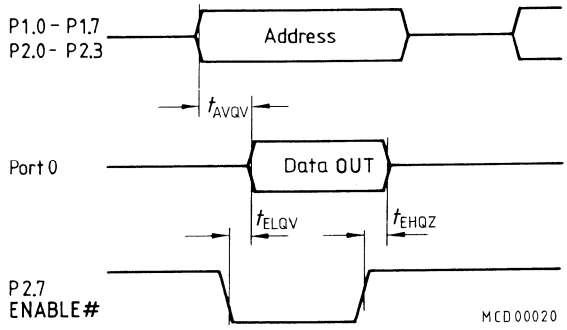
A.C. testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2 mA or sources 400 µA at voltage test levels.

ROM Verification Characteristics

T_A = 25 °C ± 5 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	$\overline{\text{ENABLE}}$ to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after $\overline{\text{ENABLE}}$	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification



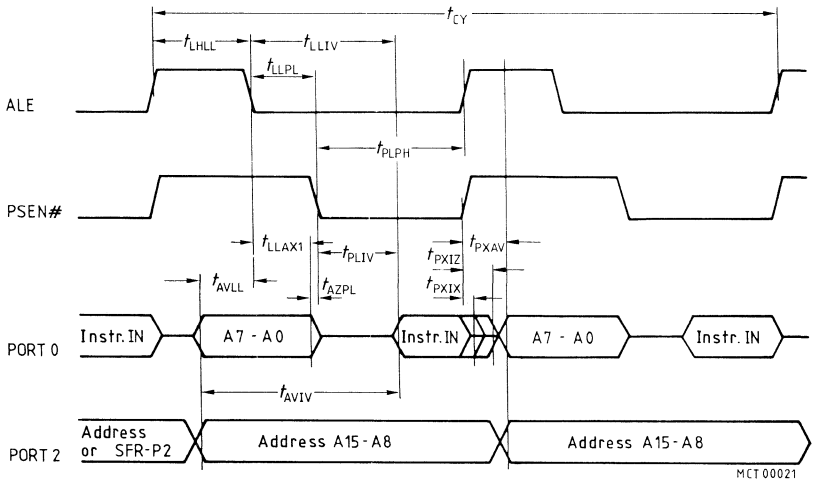
Address: P1.0–P1.7 = A0–A7
P2.0–P2.3 = A8–A11

Data: Port 0 = D0–D7

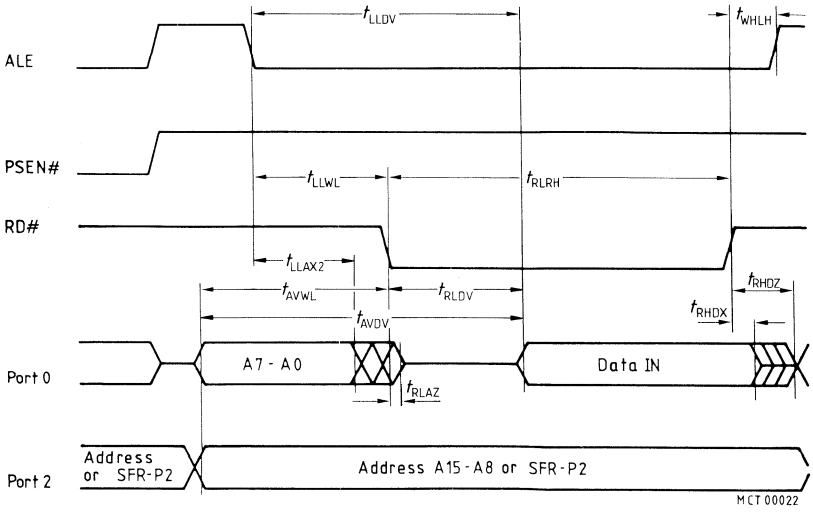
Inputs: P2.4 – P2.6, $\overline{\text{PSEN}}$ = V_{SS}
ALE, $\overline{\text{EA}}$ = V_{IH}
RST/VPD = V_{IH1}

Waveforms

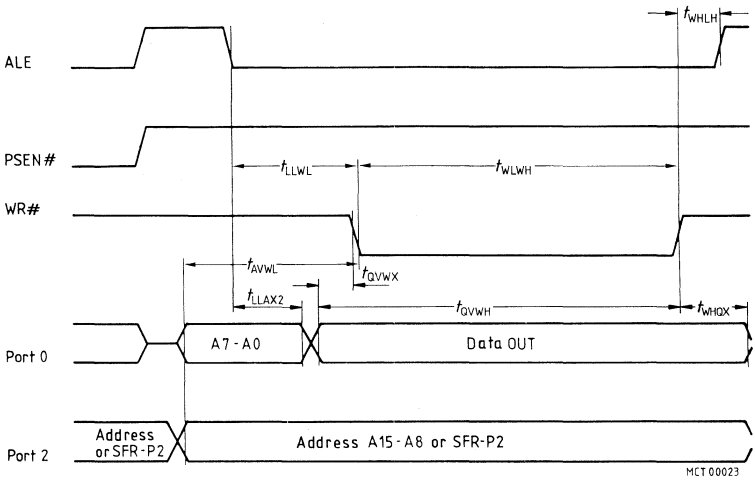
Program Memory Read Cycle



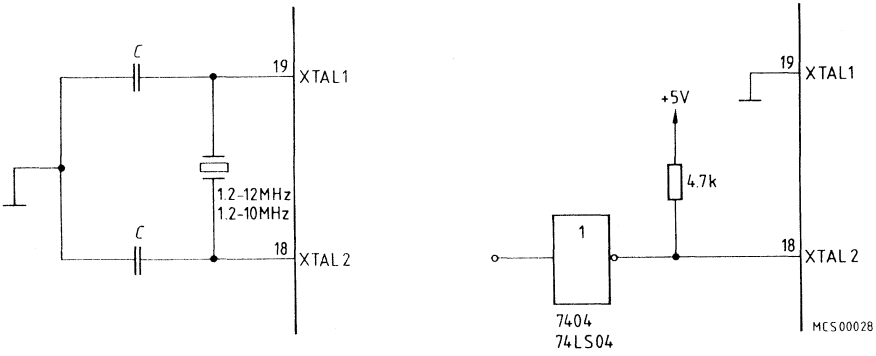
Data Memory Read Cycle



Data Memory Write Cycle



Recommended Oscillator Circuits



$C = 30\,pF \pm 10pF$

Crystal Oscillator Mode

Driving from External Source

8-Bit Single Chip Microcontroller — SAB 8052A/8032A

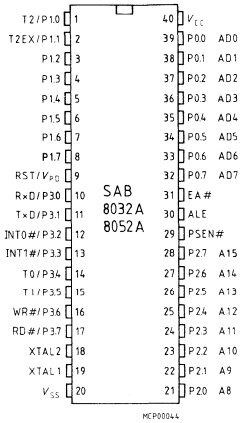
Preliminary

SAB 8052A-P(N) Microcontroller with factory-maskprogrammabel ROM
SAB 8032A-P(N) Microcontroller for external ROM

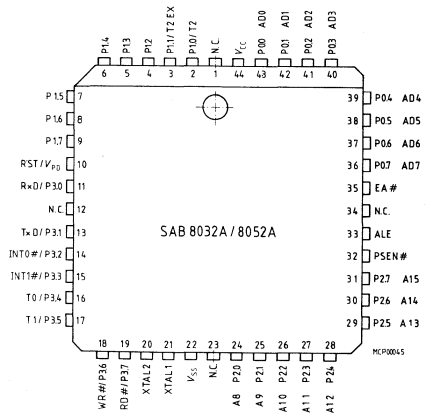
- 8 K × 8 ROM (SAB 8052A only)
- 256 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- High-performance full-duplex serial channel with flexible transmit/receive baud rate capability
- External memory expandable up to 128 Kbytes
- Boolean processor
- Most instructions execute in 1 µs
- Multiply and divide in 4 µs
- Six interrupt vectors, two priority levels
- RAM power-down supply
- P-DIP-40 and PL-CC-44 package
- Full backward compatibility with SAB 8051/8031

Pin Configuration

P-DIP-40



PL-CC-44



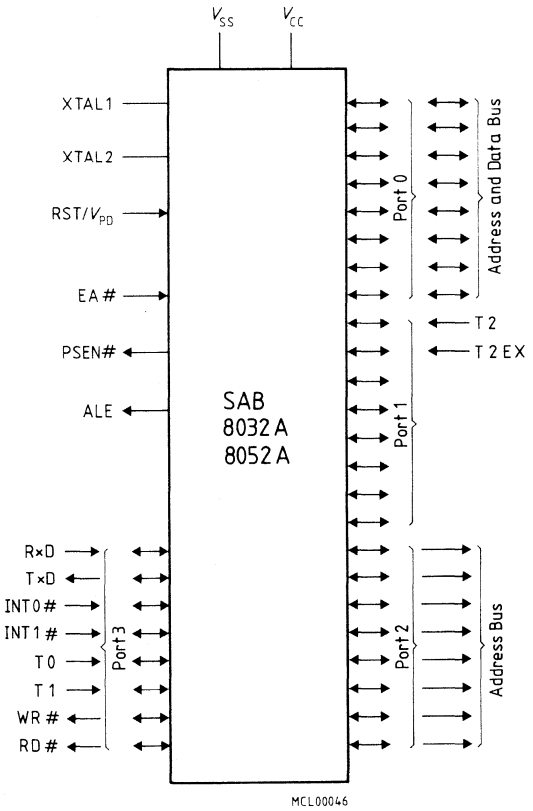
The SAB 8052A/8032A is a standalone, high-performance single-chip microcontroller fabricated in + 5 V advanced N-channel, silicon gate Siemens MYMOS technology, packaged in a 40-pin DIP or 44-pin plastic leaded chip carrier (PL-CC-44) package. It is backwardly compatible with the SAB 8051A/8031A. It provides the hardware features,

architectural enhancements, and instructions that are necessary to make it a powerful and cost-effective controller for applications requiring up to 64 Kbytes of program memory and/or up to 64 Kbytes of data memory.

The SAB 8052A contains a non-volatile 8 K × 8 read-only program memory; a volatile 256 × 8 read/write data memory; 32 I/O lines; three 16-bit timer/ counters; a six-source, two-priority-level, nested interrupt structure; a serial I/O port for either multiprocessor communications, I/O expansion, or full-duplex UART; as well as on-chip oscillator and clock circuits. The SAB 8032A is identical with the SAB 8052A, except that it lacks the program memory.

For systems that require extra capability, the SAB 8052A can be expanded using standard TTL compatible memories and the byte-oriented SAB 8080 and SAB 8085 peripherals.

Logic Symbol



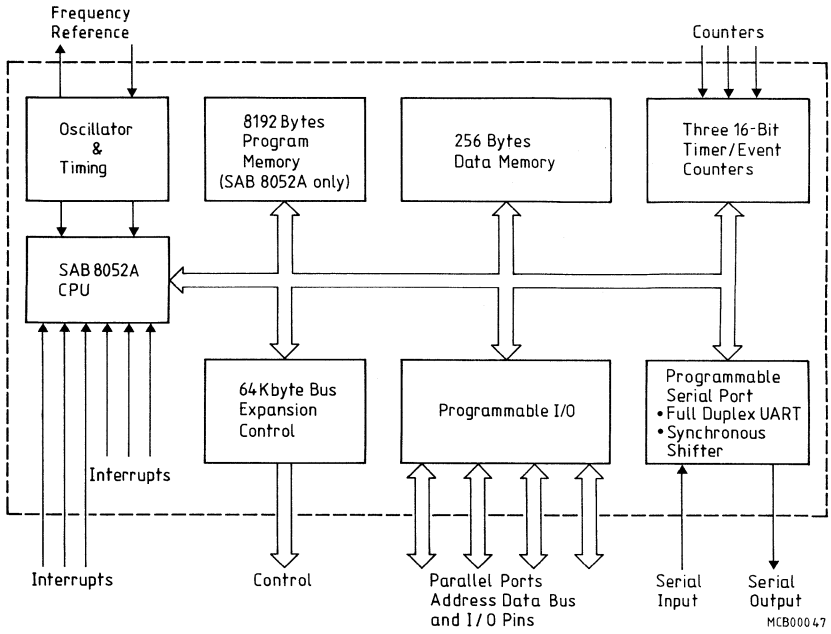
Pin Definitions and Functions

Symbol	Pin DIP-40	Pin PL-CC-44	Input (I) Output (O)	Function
P1.0-P1.7	1-8	2-9	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads. Port 1 also contains the timer 2 pins as a secondary function. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 1, as follows: – T2 (P1.0). Input to counter 2. – T2 EX (P1.1). Capture/Reload trigger of timer 2.
RST/V_{PD}	9	10	I	A high level on this pin resets the SAB 8052A. A small internal pulldown resistor permits power-on reset using only a capacitor connected to V_{CC}. If V_{PD} is held within its spec while V_{CC} drops below spec, V_{PD} will provide standby power to the RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
P3.0-P3.7	10-17	11, 13-19	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of Port 3, as follows: – RxD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TxD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – $\overline{RD}$ (P3.7). The read control signal enables external data memory to port 0.
XTAL 1 XTAL 2	19 18	21 20	I	XTAL 1 input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to V_{SS} when external source is used on XTAL 2. XTAL 2 output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0-P2.7	21-28	24-31	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.

Pin Definitions and Functions (cont'd)

Symbol	Pin		Input (I) Output (O)	Function
	DIP-40	PL-CC-44		
$\overline{PSEN}$	29	32	O	The programm store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	33	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{EA}$	31	35	I	When held at a TTL high level, the SAB 8052A executes instructions from the internal ROM when the PC is less than 8192. When held at a TTL low level, the SAB 8052A fetches all instructions from external program memory. For the SAB 8032A this pin must be tied low.
P0.0-P0.7	39-32	43-36	I/O	Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
V_{CC}	40	44	–	+ 5 V power supply during operation and program verification.
V_{SS}	20	22	–	Circuit ground potential
NC	–	1, 12 23, 34	–	No connection

Block Diagram



Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct*)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct, A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2
MOV	direct,@R	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1

*) MOV A,AAC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0 – R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is + 127/– 128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr,code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr,code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,*#data*
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr,code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,*#data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr,#data*
44	2	ORL	A,*#data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr,#data*
54	2	ANL	A,*#data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr,#data*
64	2	XRL	A,*#data*
65	2	XRL	A,*data addr*

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
66	1	XRL	A,@R0
67	1	XRL	A,@R1
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr*,*data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*,R2
8B	2	MOV	*data addr*,R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data*,*code addr*
B5	3	CJNE	A,*data addr*,*code addr*
B6	3	CJNE	@R0,#*data*,*code addr*
B7	3	CJNE	@R1,#*data*,*code addr*
B8	3	CJNE	R0,#*data*,*code addr*
B9	3	CJNE	R1,#*data*,*code addr*
BA	3	CJNE	R2,#*data*,*code addr*
BB	3	CJNE	R3,#*data*,*code addr*
BC	3	CJNE	R4,#*data*,*code addr*
BD	3	CJNE	R5,#*data*,*code addr*
BE	3	CJNE	R6,#*data*,*code addr*
BF	3	CJNE	R7,#*data*,*code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr**)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr*,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	0 to 70 °C
Storage temperature	– 65 to + 150 °C
Voltage on any pin with respect to ground (V_{SS})	– 0.5 to + 7 V
Power dissipation	2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	Limit Values		Unit	Test Condition
		min.	max.		
V_{IL}	Input low voltage	– 0.5	0.8	V	–
V_{IH}	Input high voltage (except RST/V_{PD} and XTAL 2)	2.0	V_{CC} + 0.5	V	–
V_{IH1}	Input high voltage to RST/V_{PD} for reset, XTAL 2	2.5	V_{CC} + 0.5	V	XTAL 1 to V_{SS}
V_{PD}	Power-down voltage to RST/V_{PD}	4.5	5.5	V	V_{CC} = 0 V
V_{OL}	Output low voltage, Ports 1, 2, 3	–	0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output low voltage Port 0, ALE, $\overline{PSEN}$	–	0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output high voltage, Ports 1, 2, 3	2.4	–	V	I_{OH} = – 80 µA
V_{OH1}	Output high voltage Port 0, ALE, $\overline{PSEN}$	2.4	–	V	I_{OH} = – 400 µA
I_{IL}	Logical 0 input current Ports 1, 2, 3	–	– 500	µA	V_{IL} = 0.45 V
I_{IL2}	Logical 0 input current XTAL 2	–	– 2.0	mA	XTAL 1 = V_{SS} V_{IL} = 0.45 V
I_{IH1}	Input high current to RST/V_{PD} for reset	–	500	µA	V_{IN} = V_{CC} – 1.5 V
I_{LI}	Input leakage current to port 0, $\overline{EA}$	–	± 10	µA	0 V < V_{IN} < V_{CC}
I_{CC}	Power supply current	–	175	mA	All outputs disconnected
I_{PD}	Power down current	–	15	mA	V_{CC} = 0 V
C_{IO}	Capacitance of I/O buffer	–	10	pF	f_c = 1 MHz

AC Characteristics

T_A = 0 °C to 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}$–40	–	ns
t_{AVLL}	Address setup to ALE	53	–	t_{CLCL}–30	–	ns
t_{LLAX1}	Address hold after ALE	48	–	t_{CLCL}–35	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	$4t_{CLCL}$–100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	58	–	t_{CLCL}–25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	$3t_{CLCL}$–35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	150	–	$3t_{CLCL}$–100	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}[1]	Input instruction float after $\overline{PSEN}$	–	63	–	t_{CLCL}–20	ns
t_{PXAV}[1]	Address valid after $\overline{PSEN}$	75	–	t_{CLCL}–8	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	$5t_{CLCL}$–115	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

[1]) Interfacing the SAB 8052A to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

External Data Memory Characteristics

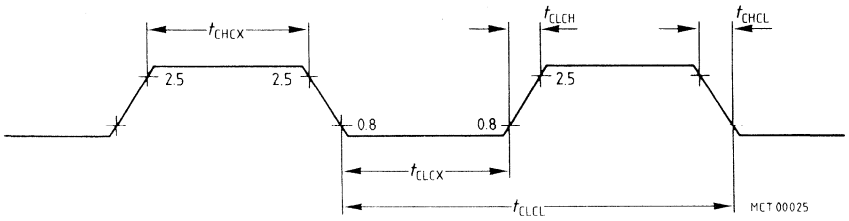
Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	132	–	$2t_{CLCL}-35$	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	252	–	$5t_{CLCL}-165$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	$2t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	517	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	585	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	33	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

External Clock Drive XTAL 2

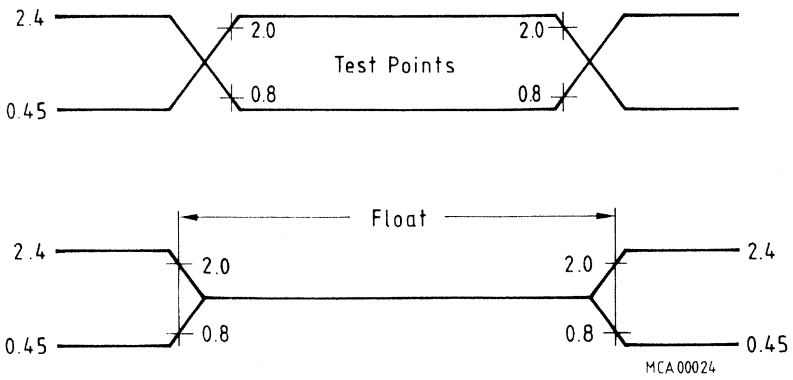
Symbol	Parameter	Limit Values		Unit
		Variable clock Freq = 1.2 MHz to 12 MHz		
		min.	max.	
t_{CLCL}	Oscillator period	83.3	833.3	ns
t_{CHCX}	High time	20	$t_{CLCL} - t_{CLCX}$	ns
t_{CLCX}	Low time	20	$t_{CLCL} - t_{CHCX}$	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

Waveforms

External Clock Cycle

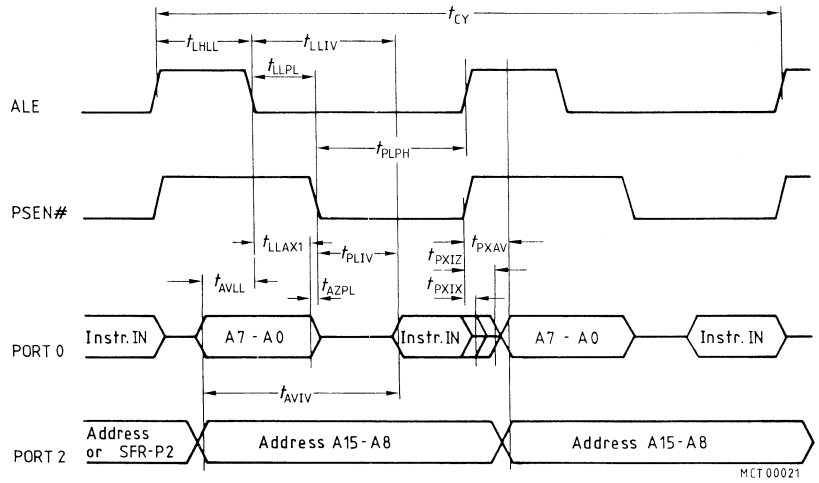


A.C. Testing Input, Output, Float Waveforms

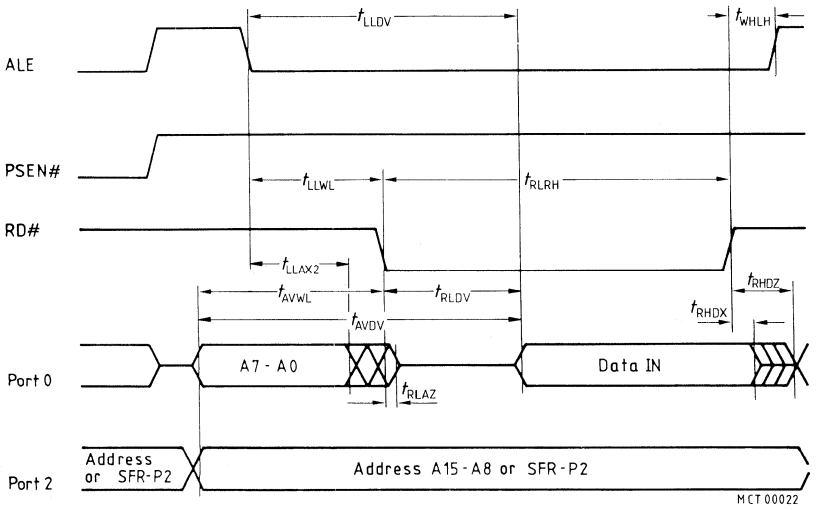


A.C. testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels.

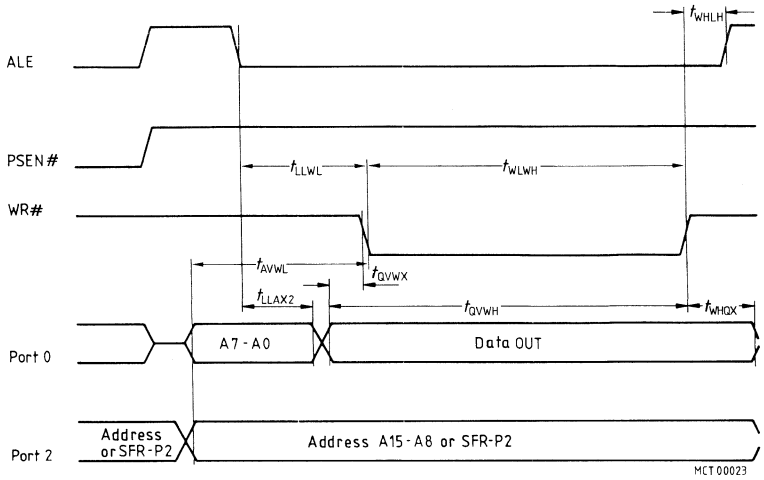
Program Memory Read Cycle



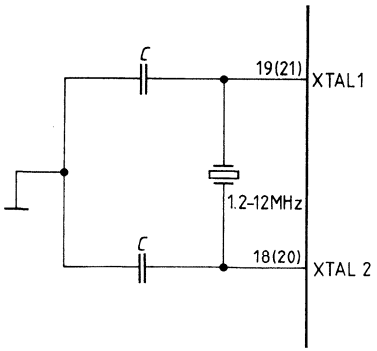
Data Memory Read Cycle



Data Memory Write Cycle

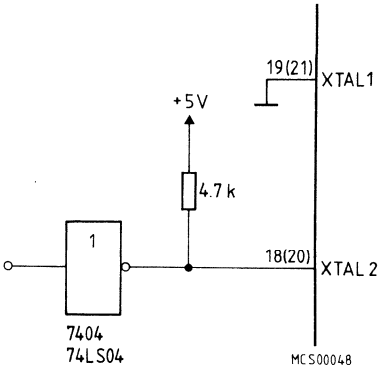


Recommended Oscillator Circuits



$C = 30\ pF \pm 10\ pF$

Crystal Oscillator Mode



Driving from External Source

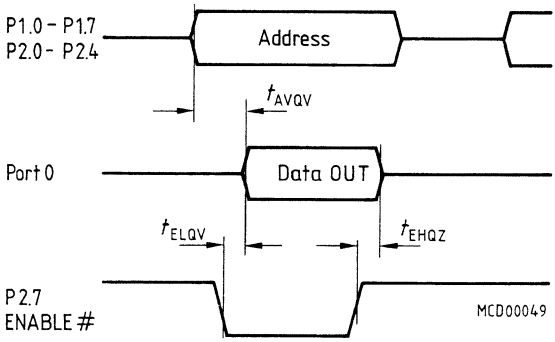
Pin numbers in (. . .) are specified for PL-CC-44 package

ROM Verification Characteristics

T_A = 25 °C ± 5 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	48 t_{CLCL}	ns
$\overline{\text{ENABLE}}$ to valid data	t_{ELQV}	–	48 t_{CLCL}	ns
Data float after $\overline{\text{ENABLE}}$	t_{EHQZ}	0	48 t_{CLCL}	ns
Oscillator frequency	1/t_{CLCL}	4	6	MHz

ROM Verification



Address: P1.0–P1.7 = A0–A7
P2.0–P2.4 = A8–A12

Data: Port 0 = D0–D7

Inputs: P2.5–P2.6, $\overline{\text{PSEN}}$ = V_{SS}
ALE, $\overline{\text{EA}}$ = TTL high level
RST/V_{PD} = V_{IH1}

Ordering Information

Type	Ordering code	Description
		8-bit single-chip microcontroller
SAB 8052A-P	Q 67120-C195	with mask-programmable ROM (P-DIP40)
SAB 8032A-P	Q 67120-C196	for external memory (P-DIP40)
SAB 8052A-N	Q 67120-C263	with mask-programmable ROM (PL-CC-44)
SAB 8032A-N	Q 67120-C264	for external memory (PL-CC-44)

SIEMENS

8-Bit Single Chip Microcontroller — SAB 8052A/8032A Ext. Temp.

Preliminary

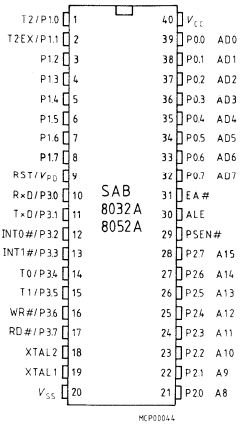
Extended Temperature Range: – 40° to + 85 °C
– 40° to + 100 °C

SAB 8052A-T40/85
SAB 8052A-T40/100 **with mask-programmable ROM**

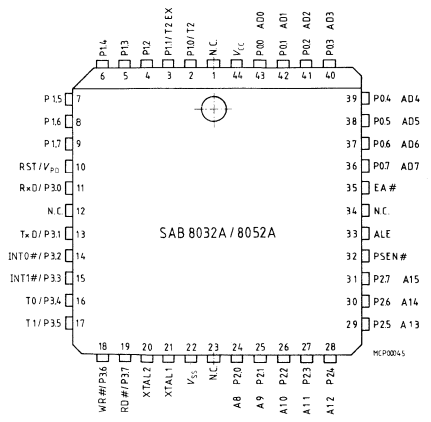
SAB 8032A-T40/85
SAB 8032A-T40/100 **for external ROM**

- 8 K × 8 ROM (SAB 8052A only)
- 256 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- High-performance full-duplex serial channel with flexible transmit/receive baud rate capability
- External memory expandable up to 128 Kbytes
- Boolean processor
- Most instructions execute in 1 µs
- Multiply and divide in 4 µs
- Six interrupt vectors, two priority levels
- RAM power-down supply
- P-DIP-40 and PL-CC-44 package
- Full backward compatibility with SAB 8051/8031

Pin Configuration
P-DIP40



PLCC44



The SAB 8052A/8032A for the two extended temperature ranges – 40 to + 85 °C and – 40 to + 100 °C is fully compatible with the standard SAB 8052A/8032A with respect to architecture, instruction set, and software portability.

The SAB 8052A/8032A is a standalone, high-performance single-chip microcontroller fabricated in + 5 V advanced N-channel, silicon gate Siemens MYMOS technology. Both extended temperature versions are available in a 40-pin plastic DIP (P-DIP-40) package: The SAB 8052A-T40/85 is also supplied in a 44-pin plastic leaded chip carrier (PL-CC-44) package.

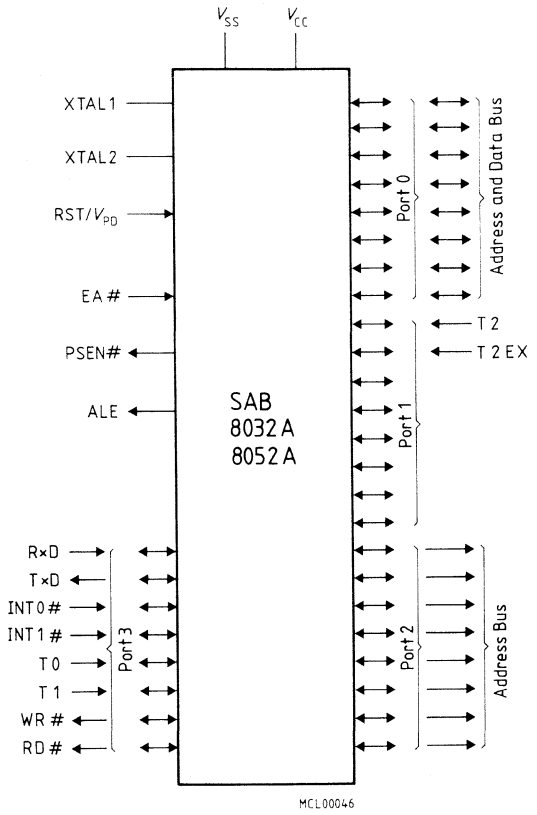
The SAB 8052A contains a non-volatile 8 K × 8 read-only program memory; a volatile 256 × 8 read/write data memory; 32 I/O lines; three 16-bit timer/counters; a six-source, two-priority-level, nested interrupt structure; a serial I/O port for either multiprocessor communications, I/O expansion, or full-duplex UART; as well as on-chip oscillator and clock circuits. The SAB 8032A is identical with the SAB 8052A, except that it lacks the program memory.

For systems that require extra capability, the SAB 8052A can be expanded using standard TTL compatible memories and the byte-oriented SAB 8080 and SAB 8085 peripherals.

Ordering Information

Type	Ordering code	Description
		8-bit single-chip microcontroller
SAB 8052A-P-T40/85	Q 67120-C247	with mask-programmable ROM (P-DIP-40)
SAB 8052A-P-T40/100	Q 67120-C248	with mask-programmable ROM (P-DIP-40)
SAB 8032A-P-T40/85	Q 67120-C235	for external memory (P-DIP-40)
SAB 8032A-P-T40/100	Q 67120-C239	for external memory (P-DIP-40)
SAB 8052A-N-T40/85	Q 67120-C368	with mask-programmable ROM (PL-CC-44)
SAB 8032A-N-T40/85	Q 67120-C367	for external memory (PL-CC-44)

Logic Symbol



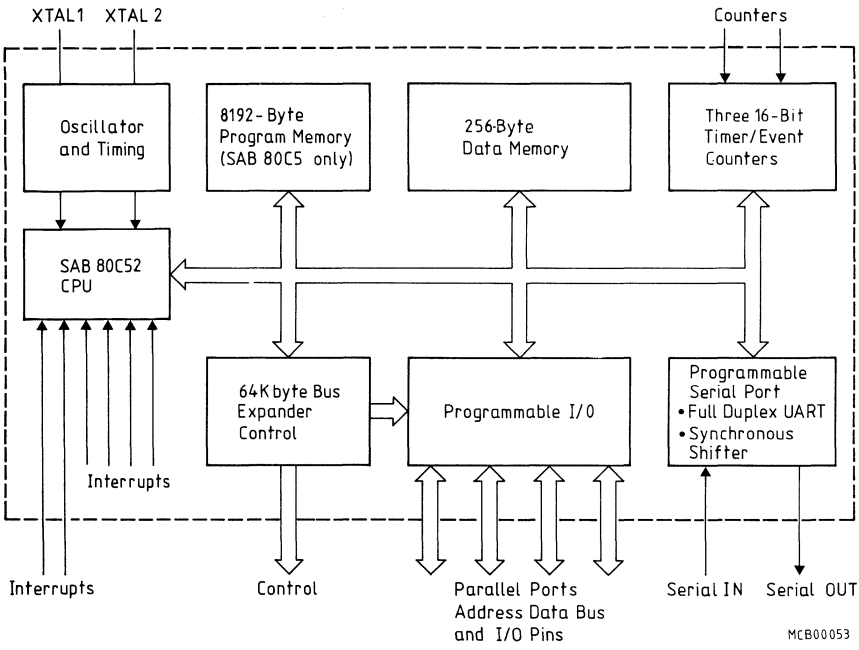
Pin Definitions and Functions

Symbol	Pin DIP40	Pin PLCC44	Input (I) Output (O)	Function
P1.0-P1.7	1-8	2-9	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads. Port 1 also contains the timer 2 pins as a secondary function. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 1, as follows: – T2 (P1.0). Input to counter 2. – T2 EX (P1.1). Capture/Reload trigger of timer 2.
RST/V_{PD}	9	10	I	A high level on this pin resets the SAB 8052A. A small internal pulldown resistor permits power-on reset using only a capacitor connected to V_{CC}. If V_{PD} is held within its spec while V_{CC} drops below spec, V_{PD} will provide standby power to the RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
P3.0-P3.7	10-17	11, 13-19	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of Port 3, as follows: – RxD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TxD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – $\overline{RD}$ (P3.7). The read control signal enables external data memory to port 0.
XTAL 1 XTAL 2	19, 18	21, 20		XTAL 1 input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to V_{SS} when external source is used on XTAL 2. XTAL 2 output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0-P2.7	21-28	24-31	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.

Pin Definitions and Functions (cont'd)

Symbol	Pin DIP40	Pin PLCC44	Input (I) Output (O)	Function
$\overline{\text{PSEN}}$	29	32	O	The programm store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	33	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{\text{EA}}$	31	35	I	When held at a TTL high level, the SAB 8052A executes instructions from the internal ROM when the PC is less than 8192. When held at a TTL low level, the SAB 8052A fetches all instructions from external program memory. For the SAB 8032A this pin must be tied low.
P0.0-P0.7	39-32	43-36	I/O	Port 0 is an 8-bit open-drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
V_{CC}	40	44	–	+ 5 V power supply during operation and program verification.
V_{SS}	20	22	–	Circuit ground potential
NC	–	1, 12 23, 34	–	No connection

Block Diagram



Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct*)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct, A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2
MOV	direct,@R	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1

*) MOV A,AAC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0 – R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is + 127/– 128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr,code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr,code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,*#data*
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr,code addr*
31	2	ACALL	*code addr*
32	1	RETI	

Hex code	Number of bytes	]Mnemo-nic	Operands
33	1	RLC	A
34	2	ADDC	A,*#data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr,#data*
44	2	ORL	A,*#data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr,#data*
54	2	ANL	A,*#data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr,#data*
64	2	XRL	A,*#data*
65	2	XRL	A,*data addr*

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
66	1	XRL	A,@R0
67	1	XRL	A,@R1
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr,data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*,R2
8B	2	MOV	*data addr*,R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data,code addr*
B5	3	CJNE	A,*data addr,code addr*
B6	3	CJNE	@R0,#*data,code addr*
B7	3	CJNE	@R1,#*data,code addr*
B8	3	CJNE	R0,#*data,code addr*
B9	3	CJNE	R1,#*data,code addr*
BA	3	CJNE	R2,#*data,code addr*
BB	3	CJNE	R3,#*data,code addr*
BC	3	CJNE	R4,#*data,code addr*
BD	3	CJNE	R5,#*data,code addr*
BE	3	CJNE	R6,#*data,code addr*
BF	3	CJNE	R7,#*data,code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr**)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr*,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	– 40 to + 85 °C for -T40/85
	– 40 to + 100 °C for -T40/100
Storage temperature	– 65 to + 150 °C
Voltage on any pin with respect to ground (V_{SS})	– 0.5 to + 7 V
Power dissipation	2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V; T_A = – 40 to + 85 °C for -T40/85;
T_A = – 40 to + 100 °C for -T40/100;

Symbol	Parameter	Limit Values		Unit	Test Condition
		min.	max.		
V_{IL}	Input low voltage	– 0.5	0.8	V	–
V_{IH}	Input high voltage (except RST/V_{PD} and XTAL 2)	2.0	V_{CC} + 0.5	V	–
V_{IH1}	Input high voltage to RST/V_{PD} for reset, XTAL 2	2.5	V_{CC} + 0.5	V	XTAL 1 to V_{SS}
V_{PD}	Power-down voltage to RST/V_{PD}	4.5	5.5	V	V_{CC} = 0 V
V_{OL}	Output low voltage, Ports 1, 2, 3	–	0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output low voltage Port 0, ALE, $\overline{PSEN}$	–	0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output high voltage, Ports 1, 2, 3	2.4	–	V	I_{OH} = – 80 µA
V_{OH1}	Output high voltage Port 0, ALE, $\overline{PSEN}$	2.4	–	V	I_{OH} = – 400 µA
I_{IL}	Logical 0 input current Ports 1, 2, 3	–	– 500	µA	V_{IL} = 0.45 V
I_{IL2}	Logical 0 input current XTAL 2	–	– 2.5	mA	XTAL 1 = V_{SS} V_{IL} = 0.45 V
I_{IH1}	Input high current to RST/V_{PD} for reset	–	500	µA	V_{IN} = V_{CC} – 1.5 V
I_{LI}	Input leakage current to port 0, $\overline{EA}$	–	± 10	µA	0 V < V_{IN} < V_{CC}
I_{CC}	Power supply current	–	175	mA	All outputs disconnected
I_{PD}	Power down current	–	15	mA	V_{CC} = 0 V
C_{IO}	Capacitance of I/O buffer	–	10	pF	f_c = 1 MHz

AC Characteristics for T40/85

V_{CC} = 5 V ± 10%; V_{SS} = 0 V; T_A = – 40° to + 85 °C
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}$–40	–	ns
t_{AVLL}	Address setup to ALE	53	–	t_{CLCL}–30	–	ns
t_{LLAX1}	Address hold after ALE	48	–	t_{CLCL}–35	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	$4t_{CLCL}$–100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	58	–	t_{CLCL}–25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	$3t_{CLCL}$–35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	150	–	$3t_{CLCL}$–100	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}[1]	Input instruction float after $\overline{PSEN}$	–	63	–	t_{CLCL}–20	ns
t_{PXAV}[1]	Address valid after $\overline{PSEN}$	75	–	t_{CLCL}–8	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	$5t_{CLCL}$–115	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

[1]) Interfacing the SAB 8052A to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

External Data Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	132	–	$2t_{CLCL}-35$	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	252	–	$5t_{CLCL}-165$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	$2t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	517	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	585	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	33	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

AC Characteristics for T40/100

V_{CC} = 5 V ± 10%; V_{SS} = 0 V; T_A = – 40° to +100 °C;
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		10 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 10 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	160	–	$2t_{CLCL}$–40	–	ns
t_{AVLL}	Address setup to ALE	70	–	t_{CLCL}–30	–	ns
t_{LLAX1}	Address hold after ALE	65	–	t_{CLCL}–35	–	ns
t_{LLIV}	ALE to valid instruction in	–	300	–	$4t_{CLCL}$–100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	75	–	t_{CLCL}–25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	265	–	$3t_{CLCL}$–35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	200	–	$3t_{CLCL}$–100	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}[1]	Input instruction float after $\overline{PSEN}$	–	80	–	t_{CLCL}–20	ns
t_{PXAV}[1]	Address valid after $\overline{PSEN}$	92	–	t_{CLCL}–8	–	ns
t_{AVIV}	Address to valid instruction in	–	385	–	$5t_{CLCL}$–115	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

[1]) Interfacing the SAB 8052A to devices with float times up to 92 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

External Data Memory Characteristics

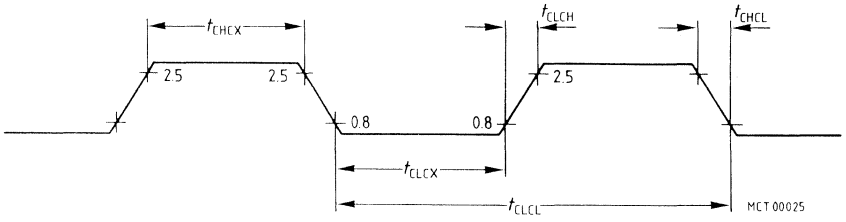
Symbol	Parameter	Limit Values				Unit
		10 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 10 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	500	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	500	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	165	–	$2t_{CLCL}-35$	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	335	–	$5t_{CLCL}-165$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	130	–	$2t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	650	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	735	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	250	350	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	270	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	60	140	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{DVWX}	Data valid to $\overline{WR}$ transition	50	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	550	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	50	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

External Clock Drive XTAL 2

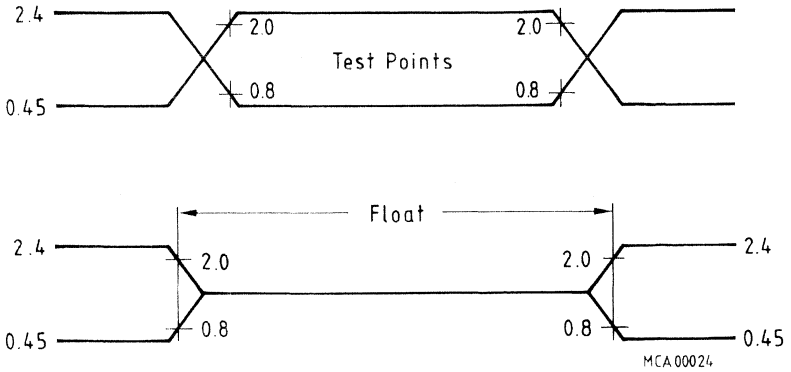
Symbol	Parameter	Limit Values		Unit
		Variable clock Freq = 1.2 MHz to 12 MHz (T40/85) Freq = 1.2 MHz to 10 MHz		
		min.	max.	
t_{CLCL}	Oscillator period T40/85 T40/100	83.3 100	833.3	ns
t_{CHCX}	High time	20	$t_{CLCL} - t_{CLCX}$	ns
t_{CLCX}	Low time	20	$t_{CLCL} - t_{CHCX}$	ns
t_{CLCH}	Rise time	–	20	ns
t_{TCHCL}	Fall time	–	20	ns

Waveforms

External Clock Cycle



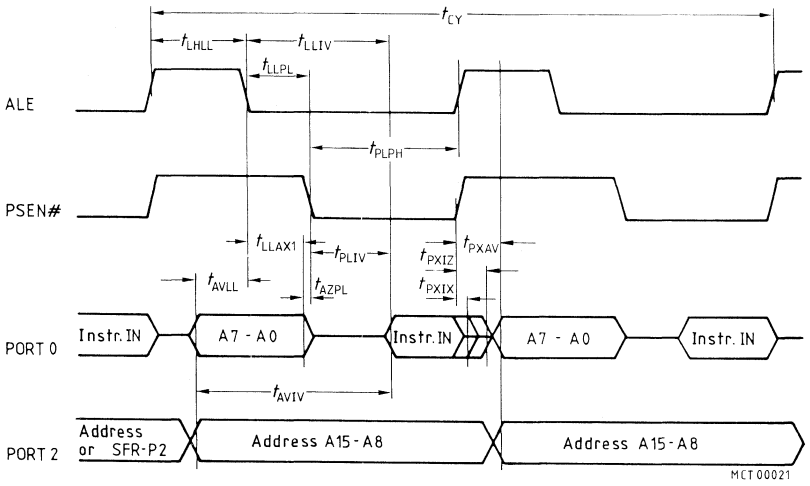
A.C. Testing Input, Output, Float Waveforms



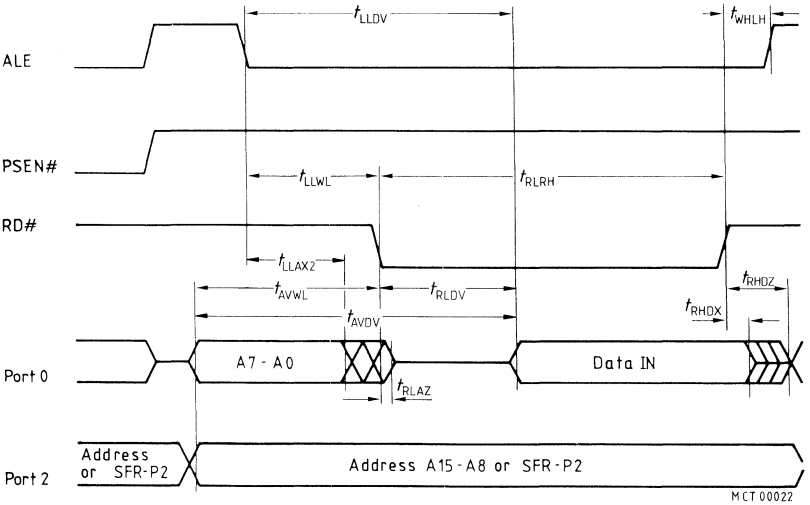
A.C. testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point where a P0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels.

Waveforms

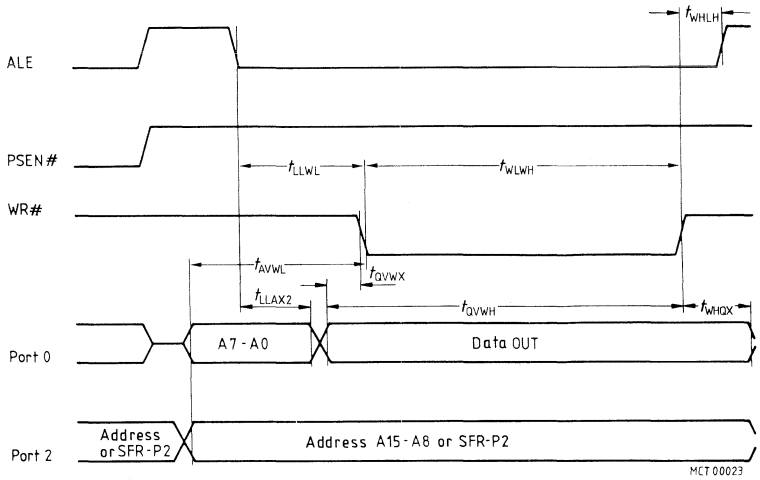
Program Memory Read Cycle



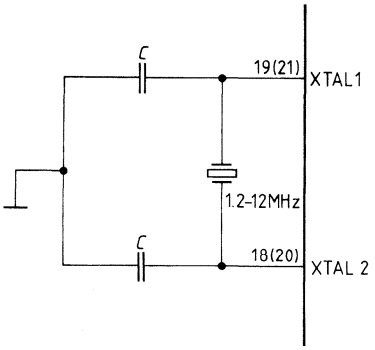
Data Memory Read Cycle



Data Memory Write Cycle

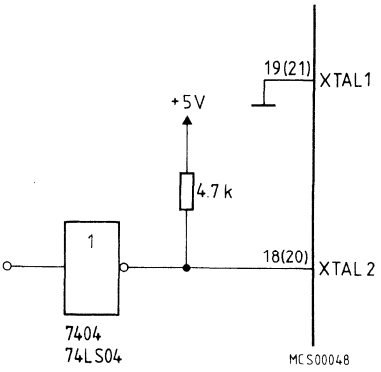


Recommended Oscillator Circuits



$C = 30\ pF \pm 10\ pF$

Crystal Oscillator Mode



Driving from External Source

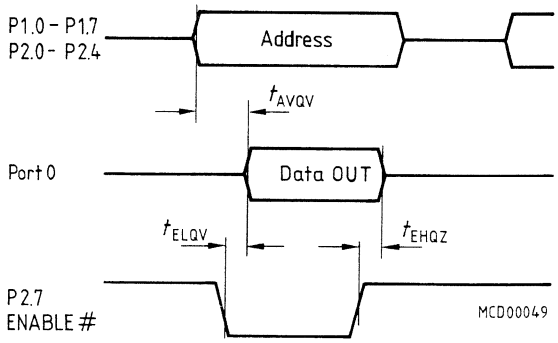
Pin numbers in (. . .) are specified for PLCC44 package

ROM Verification Characteristics

T_A = 25 °C ± 5 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	$\overline{\text{ENABLE}}$ to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after $\overline{\text{ENABLE}}$	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification



Address: P1.0–P1.7 = A0–A7
P2.0–P2.4 = A8–A12

Data: Port 0 = D0–D7

Inputs: P2.5–P2.6, $\overline{\text{PSEN}}$ = V_{SS}
ALE, $\overline{\text{EA}}$ = V_{IH}
RST/V_{PD} = V_{IH1}

SIEMENS

8-Bit Single-Chip Microcontroller

SAB 8052B/8032B
SAB 8052B-16/8032B-16, SAB 8032-20

Preliminary

SAB 8052B Microcontroller with factory-maskprogrammable ROM
SAB 8032B Microcontroller for external ROM

- SAB 8052B/8032B, 12 MHz operation
  SAB 8052B-16/8032B-16, 16 MHz operation
  SAB 8032B-20, 20 MHz operation
- 8 K × 8 ROM (SAB 8052B only)
- 256 K × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- High-performance full-duplex serial channel with flexible transmit/receive baud rate capability
- External memory expandable up to 128 Kbytes
- Boolean processor
- Most instructions execute in 1 µs/750 ns/600 ns
- Multiply and divide in 4 µs/3 µs/2.4 4 µs
- Six interrupt vectors, two priority levels
- RAM power-down supply
- Packages P-DIP-40 and PL-CC-44
- Full backward compatibility with SAB 8051/8031

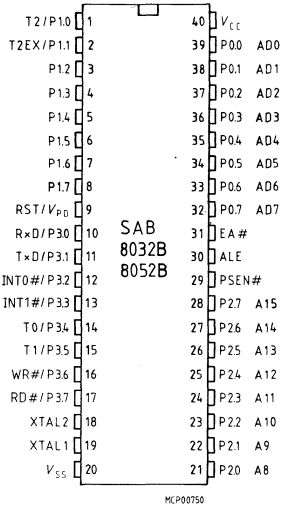
The SAB 8052B/8032B is a standalone, high-performance single-chip microcontroller fabricated in + 5 V advanced N-channel, silicon-gate Siemens MYMOS technology, packaged in a 40-pin plastic dual-in-line package (P-DIP-40) or 44-pin plastic leaded chip carrier (PL-CC-44) package. It is backwardly compatible with the SAB 8051A/8031A and provides the hardware features, architectural enhancements, and instructions that are necessary to make it a powerful and cost-effective controller for applications requiring up to 64 Kbytes of program memory and/or up to 64 Kbytes of data memory.

The SAB 8052B contains a non-volatile 8 K × 8 read-only program memory, a volatile 256 × 8 read/write data memory, 32 I/O lines, three 16-bit timer/counters, a six-source, two-priority-level nested interrupt structure, a serial I/O port for either multiprocessor communications, I/O expansion, or full-duplex UART, as well as on-chip oscillator and clock circuits. The SAB 8032B is identical with the SAB 8052B, except that it lacks the program memory.

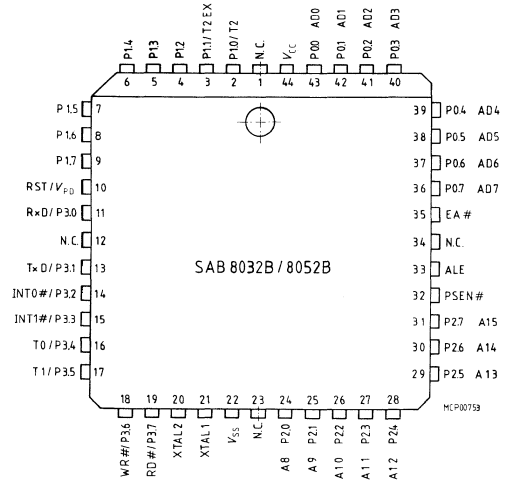
For systems that require extra capability, the SAB 8052B can be expanded using standard TTL compatible memories and the byte-oriented SAB 8080 and SAB 8085 peripherals.

Pin Configuration

P-DIP-40



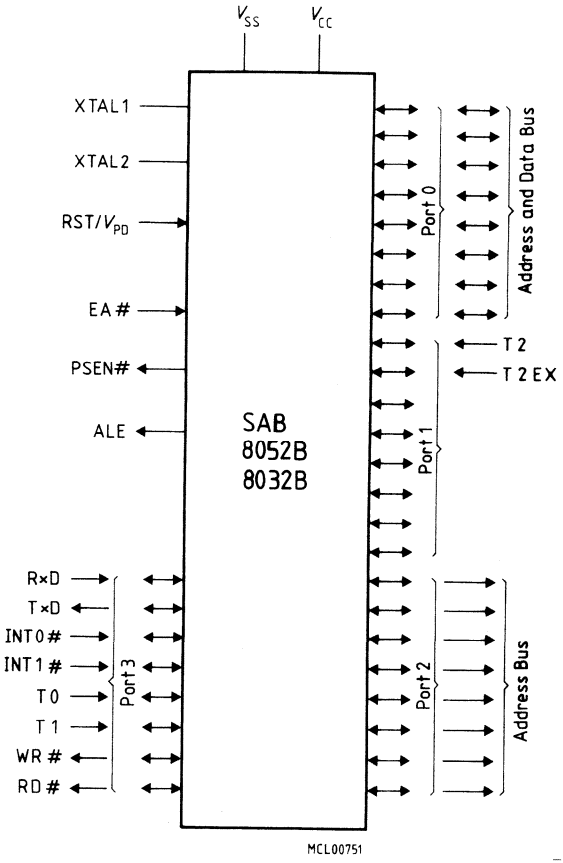
PL-CC-44



Ordering Information

Type	Ordering code	Package	Description (8-bit single-chip microcontroller)
SAB 8052B-P	Q 67120-C420	P-DIP-40	with mask-programmable ROM, 12 MHz
SAB 8032B-P	Q 67120-C419	P-DIP-40	for external memory, 12 MHz
SAB 8052B-16-P	Q 67120-C422	P-DIP-40	with mask-programmable ROM, 16 MHz
SAB 8032B-16-P	Q 67120-C421	P-DIP-40	for external memory, 16 MHz
SAB 8032B-20-P	Q 67120-C471	P-DIP-40	for external memory, 20 MHz
SAB 8052B-N	Q 67120-C424	PL-CC-44	with mask-programmable ROM, 12 MHz
SAB 8032B-N	Q 67120-C423	PL-CC-44	for external memory, 12 MHz
SAB 8052B-16-N	Q 67120-C426	PL-CC-44	with mask-programmable ROM, 16 MHz
SAB 8032B-16-N	Q 67120-C425	PL-CC-44	for external memory, 16MHz
SAB 8032B-20-N	Q 67120-C472	PL-CC-44	for external memory, 20 MHz

Logic Symbol



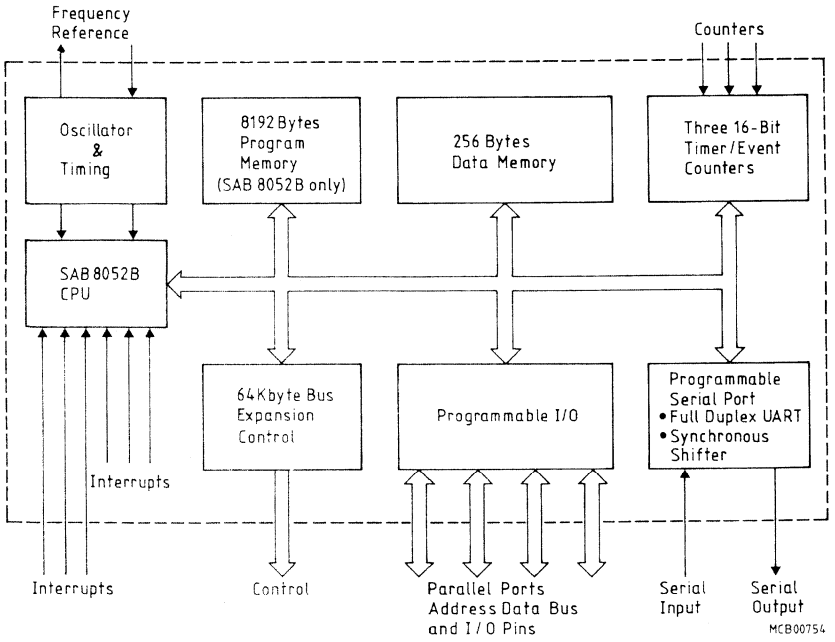
Pin Definitions and Functions

Symbol	Pins		Input (I) Output (O)	Function
	P-DIP-40	PL-CC-44		
P1.0-P1.7	1-8	2-9	I/O	**PORT 1** is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads. Port 1 also contains the timer 2 pins as a secondary function. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 1, as follows: – T2 (P1.0). Input to counter 2. – T2 (EX (P1.1). Capture/Reload trigger of timer 2.
RST/V_{PD}	9	10	I	**RESET** input. A high level on this pin resets the SAB 8052B. A small internal pulldown resistor permits power-on reset using only a capacitor connected to V_{CC}. If V_{PD} is held within its spec while V_{CC} drops below spec, V_{PD} will provide standby power to the RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
P3.0-P3.7	10-17	11 13-19	I/O	**PORT 3** is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and RD# and WR# pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of port 3, as follows: – RxD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TxD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – INTO# (P3.2). Interrupt 0 input or gate control input for counter 0. – INT1# (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – WR# (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – RD# (P3.7). The read control signal enables external data memory to port 0.
XTAL1 XTAL2	19 18	21 20	I	**XTAL 1** input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to V_{SS} when external source is used on XTAL 2. **XTAL 2** output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0-P2.7	21-28	24-31	I/O	**PORT 2** is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.

Pin Definitions and Functions (cont'd)

Symbol	Pins		Input (I) Output (O)	Function
	P-DIP-40	PL-CC-44		
PSEN#	29	32	O	The **Program Store Enable#** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	33	O	Provides **Address Latch Enable** output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
EA#	31	35	I	**External Access#** enable. When held at a TTL high level, the SAB 8052B executes instructions from the internal ROM when the PC is less than 8192. When held at a TTL low level, the SAB 8052B fetches all instructions from external program memory. For the SAB 8032B this pin must be tied low.
P0.0-P0.7	39-32	43-36	I/O	**Port 0** is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
V_{CC}	40	44	–	+ 5 V **Power Supply** during operation and program verification.
V_{SS}	20	22	–	Circuit **Ground** potential
NC	–	1,12, 23,34	–	**No Connection**

Block Diagram



Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct*)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct, A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2
MOV	direct,@R	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Compare immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Compare immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Compare immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Notes on data addressing modes:

Rn – Working register R0 – R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is + 127/– 128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr,code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr,code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,*#data*
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr,code addr*
31	2	ACALL	*code addr*
32	1	RETI	

Hex code	Number of bytes	Mnemonic	Operands
33	1	RLC	A
34	2	ADDC	A,*#data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R6
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr,#data*
44	2	ORL	A,*#data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr,#data*
54	2	ANL	A,*#data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr,#data*
64	2	XRL	A,*#data*
65	2	XRL	A,*data addr*

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
66	1	XRL	A,@R0
67	1	XRL	A,@R1
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr*,*data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*,R2
8B	2	MOV	*data addr*,R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data*,*code addr*
B5	3	CJNE	A,*data addr*,*code addr*
B6	3	CJNE	@R0,#*data*,*code addr*
B7	3	CJNE	@R1,#*data*,*code addr*
B8	3	CJNE	R0,#*data*,*code addr*
B9	3	CJNE	R1,#*data*,*code addr*
BA	3	CJNE	R2,#*data*,*code addr*
BB	3	CJNE	R3,#*data*,*code addr*
BC	3	CJNE	R4,#*data*,*code addr*
BD	3	CJNE	R5,#*data*,*code addr*
BE	3	CJNE	R6,#*data*,*code addr*
BF	3	CJNE	R7,#*data*,*code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr**)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr*,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias ..... 0 to + 70 °C
Storage temperature ..... – 65 to + 150 °C
Voltage on any pin with respect to ground (V_{SS}) ..... – 0.5 to + 7 V
Power dissipation ..... 2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	Limit Values		Unit	Test Condition
		min.	max.		
V_{IL}	Input low voltage	– 0.5	0.8	V	–
V_{IH}	Input high voltage (except RST/V_{PD} and XTAL 2)	2.0	V_{CC} + 0.5	V	–
V_{IH1}	Input high voltage to RST/V_{PD} for reset, XTAL 2	2.5	V_{CC} + 0.5	V	XTAL1 to V_{SS}
V_{PD}	Power down voltage to RST/V_{PD}	4.5	5.5	V	V_{CC} = 0 V
V_{OL}	Output low voltage Ports 1, 2, 3	–	0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output low voltage Port 0, ALE, PSEN#	–	0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output high voltage Ports 1, 2, 3	2.4	–	V	I_{OH} = – 80 µA
V_{OH1}	Output high voltage Port 0, ALE, PSEN#	2.4	–	V	I_{OH} = – 400 µA
I_{IL}	Logical 0 input current Ports 1, 2, 3	–	– 500	µA	V_{IL} = 0.45 V
I_{IL2}	Logical 0 input current XTAL 2	–	– 3.2	mA	XTAL 1 = V_{SS} V_{IL} = 0.45 V
I_{IH1}	Input high current to RST/V_{PD} for reset	–	500	µA	V_{IN} = V_{CC} – 1.5 V
I_{LI}	Input leakage current to port 0, EA#	–	± 10	µA	0 V < V_{IN} < V_{CC}
I_{CC}	Power supply current	–	175	mA	All outputs disconnected
I_{PD}	Power down current	–	15	mA	V_{CC} = 0 V
C_{IO}	Capacitance of I/O buffer	–	10	pF	f_c = 1 MHz

AC Characteristics for SAB 8052B/8032B, 12 MHz

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V
(C_L for port 0, ALE and PSEN# outputs = 100 pF; C_L for all other outputs = 80 pF)

Symbol	Parameter	Limit Values				Unit
		clock 12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}-40$	–	ns
t_{AVLL}	Address setup to ALE	53	–	$t_{CLCL}-30$	–	ns
t_{LLAX1}	Address hold after ALE	48	–	$t_{CLCL}-35$	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	$4t_{CLCL}-100$	ns
t_{LLPL}	ALE to PSEN#	58	–	$t_{CLCL}-25$	–	ns
t_{PLPH}	PSEN# pulse width	215	–	$3t_{CLCL}-35$	–	ns
t_{PLIV}	PSEN# to valid instruction in	–	150	–	$3t_{CLCL}-100$	ns
t_{PXIX}	Input instruction hold after PSEN#	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float after PSEN#	–	63	–	$t_{CLCL}-20$	ns
t_{PXAV}*)	Address valid after PSEN#	75	–	$t_{CLCL}-8$	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	$5t_{CLCL}-115$	ns
t_{AZPL}	Address float to PSEN#	0	–	0	–	ns

*) Interfacing the SAB 8052B to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for SAB 8052B/8032B, 12 MHz (cont'd)

Symbol	Parameter	Limit Values				Unit
		Clock 12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
External Data Memory Characteristics						
t_{RLRH}	RD# pulse width	400	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	WR# pulse width	400	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	132	–	$2t_{CLCL}-35$	–	ns
t_{RLDV}	RD# to valid data in	–	252	–	$5t_{CLCL}-165$	ns
t_{RHDX}	Data hold after RD#	0	–	0	–	ns
t_{RHDZ}	Data float after RD#	–	97	–	$2t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	517	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	585	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to WR# or RD#	200	300	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to WR# or RD#	203	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	WR# or RD# high to ALE high	43	123	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{QVWX}	Data valid to WR# transition	33	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before WR#	433	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after WR#	33	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after RD#	–	0	–	0	ns
External Clock Drive XTAL2						
t_{CLCL}	Oscillator period	–	–	83.3	833.3	ns
t_{CHCX}	High time	–	–	20	$t_{CLCL}-t_{CLCX}$	ns
t_{CLCX}	Low time	–	–	20	$t_{CLCL}-t_{CHCX}$	ns
t_{CLCH}	Rise time	–	–	–	20	ns
t_{CHCL}	Fall time	–	–	–	20	ns

AC Characteristics for SAB 8052B-16/8032B-16

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V
(C_L for port 0, ALE and PSEN# outputs = 100 pF; C_L for all other outputs = 80 pF)

Symbol	Parameter	Limit Values				Unit
		Clock 16 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 16 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
t_{LHLL}	ALE pulse width	85	–	$2t_{CLCL}$–40	–	ns
t_{AVLL}	Address setup to ALE	33	–	t_{CLCL}–30	–	ns
t_{LLAX1}	Address hold after ALE	28	–	t_{CLCL}–35	–	ns
t_{LLIV}	ALE to valid instruction in	–	150	–	$4t_{CLCL}$–100	ns
t_{LLPL}	ALE to PSEN#	38	–	t_{CLCL}–25	–	ns
t_{PLPH}	PSEN# pulse width	153	–	$3t_{CLCL}$–35	–	ns
t_{PLIV}	PSEN# to valid instruction in	–	88	–	$3t_{CLCL}$–100	ns
t_{PXIX}	Input instruction hold after PSEN#	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float afterPSEN#	–	48	–	t_{CLCL}–15	ns
t_{PXAV}*)	Address valid after PSEN#	60	–	t_{CLCL}–3	–	ns
t_{AVIV}	Address to valid instruction in	–	223	–	$5t_{CLCL}$–90	ns
t_{AZPL}	Address float to PSEN#	0	–	0	–	ns

*) Interfacing the SAB 8052B-16 to devices with float times up to 55 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for SAB 8052B-16 (cont'd)

Symbol	Parameter	Limit Values				Unit
		Clock 16 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 16 MHz		
		min.	max.	min.	max.	
External Data Memory Characteristics						
t_{RLRH}	RD# pulse width	275	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	WR# pulse width	275	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	90	–	$2t_{CLCL}-35$	–	ns
t_{RLDV}	RD# to valid data in	–	148	–	$5t_{CLCL}-165$	ns
t_{RHDX}	Data hold after RD#	0	–	0	–	ns
t_{RHDZ}	Data float after RD#	–	55	–	$2t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	350	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	398	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to WR# or RD#	138	238	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to WR# or RD#	120	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	WR# or RD# high to ALE high	23	103	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{QVWX}	Data valid to WR# transition	13	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before WR#	288	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after WR#	13	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after RD#	–	0	–	0	ns
External Clock Drive XTAL2						
t_{CLCL}	Oscillator period	–	–	62.5	833.3	ns
t_{CHCX}	High time	–	–	15	$t_{CLCL}-t_{CLCX}$	ns
t_{CLCX}	Low time	–	–	15	$t_{CLCL}-t_{CHCX}$	ns
t_{CLCH}	Rise time	–	–	–	15	ns
t_{CHCL}	Fall time	–	–	–	15	ns

AC Characteristics for SAB 8032B-20

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V
(C_L for port 0, ALE and PSEN# outputs = 100 pF; C_L for all other outputs = 80 pF)

Symbol	Parameter	Limit Values				Unit
		Clock 20 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 20 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
t_{LHLL}	ALE pulse width	60	–	$2t_{CLCL}$–40	–	ns
t_{AVLL}	Address setup to ALE	20	–	t_{CLCL}–30	–	ns
t_{LLAX1}	Address hold after ALE	20	–	t_{CLCL}–30	–	ns
t_{LLIV}	ALE to valid instruction in	–	100	–	$4t_{CLCL}$–100	ns
t_{LLPL}	ALE to PSEN#	25	–	t_{CLCL}–25	–	ns
t_{PLPH}	PSEN# pulse width	115	–	$3t_{CLCL}$–35	–	ns
t_{PLIV}	PSEN# to valid instruction in	–	75	–	$3t_{CLCL}$–75	ns
t_{PXIX}	Input instruction hold after PSEN#	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float afterPSEN#	–	40	–	t_{CLCL}–10	ns
t_{PXAV}*)	Address valid after PSEN#	47	–	t_{CLCL}–3	–	ns
t_{AVIV}	Address to valid instruction in	–	190	–	$5t_{CLCL}$–60	ns
t_{AZPL}	Address float to PSEN#	0	–	0	–	ns

*) Interfacing the SAB 8032B-20 to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for SAB 8032B-20 (cont'd)

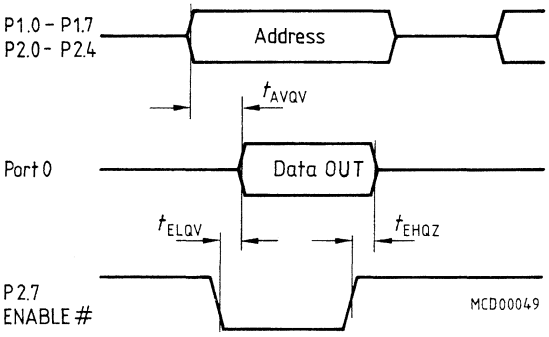
Symbol	Parameter	Limit Values				Unit
		Clock 20 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 20 MHz		
		min.	max.	min.	max.	
External Data Memory Characteristics						
t_{RLRH}	RD# pulse width	200	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	WR# pulse width	200	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	70	–	$2t_{CLCL}-30$	–	ns
t_{RLDV}	RD# to valid data in	–	100	–	$5t_{CLCL}-150$	ns
t_{RHDX}	Data hold after RD#	0	–	0	–	ns
t_{RHDZ}	Data float after RD#	–	40	–	$2t_{CLCL}-60$	ns
t_{LLDV}	ALE to valid data in	–	250	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	285	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to WR# or RD#	100	200	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to WR# or RD#	70	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	WR# or RD# high to ALE high	20	80	$t_{CLCL}-30$	$t_{CLCL}+30$	ns
t_{QVWX}	Data valid to WR# transition	5	–	$t_{CLCL}-45$	–	ns
t_{QVWH}	Data setup before WR#	200	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after WR#	10	–	$t_{CLCL}-40$	–	ns
t_{RLAZ}	Address float after RD#	–	0	–	0	ns
External Clock Drive XTAL2						
t_{CLCL}	Oscillator period	–	–	50	833.3	ns
t_{CHCX}	High time	–	–	15	$t_{CLCL}-t_{CLCX}$	ns
t_{CLCX}	Low time	–	–	15	$t_{CLCL}-t_{CHCX}$	ns
t_{CLCH}	Rise time	–	–	–	15	ns
t_{CHCL}	Fall time	–	–	–	15	ns

ROM Verification Characteristics for SAB 8052B

T_A = 25 °C ± 5 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	ENABLE# to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after ENABLE#	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification

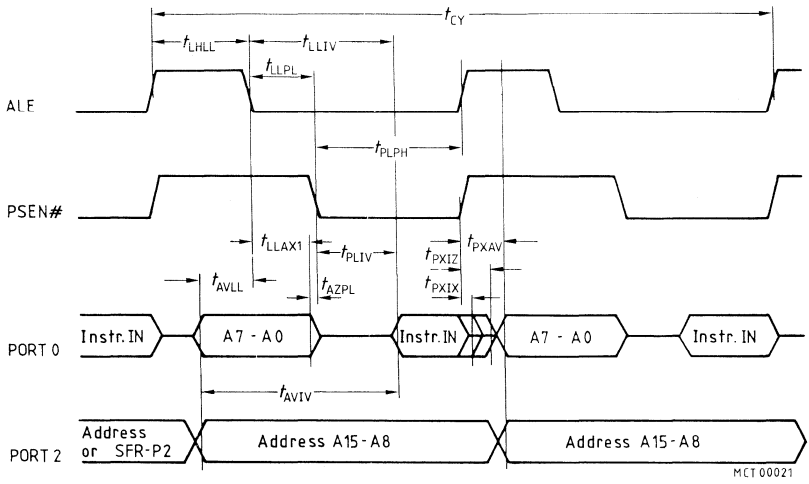


Address: P1.0–P1.7 = A0–A7
P2.0–P2.4 = A8–A12

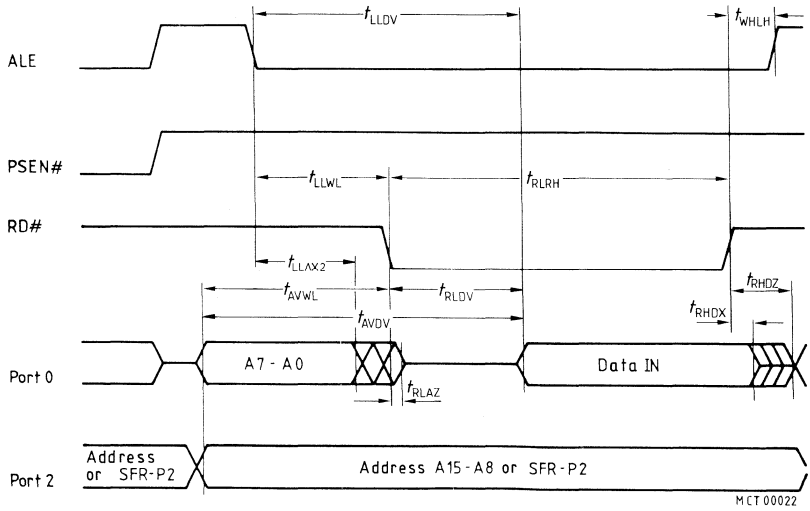
Data: Port 0 = D0–D7

Inputs: P2.5 – P2.6, PSEN# = V_{SS}
ALE, EA# = V_{IH}
R_{ST}/V_{PD} = V_{IH1}

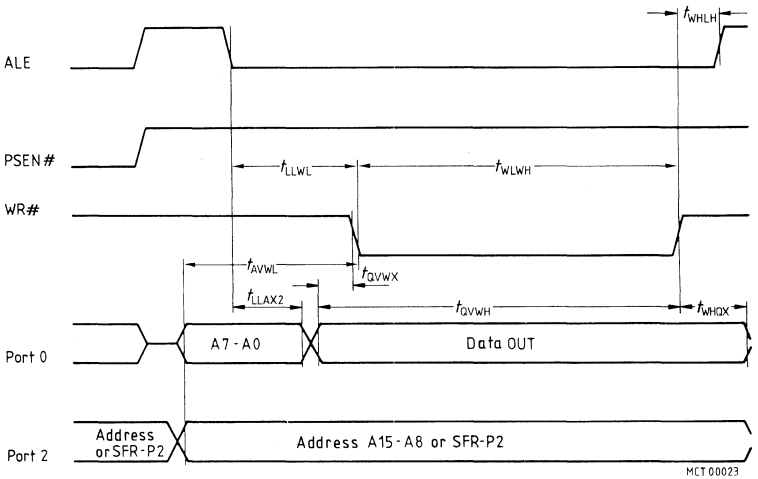
Program Memory Read Cycle



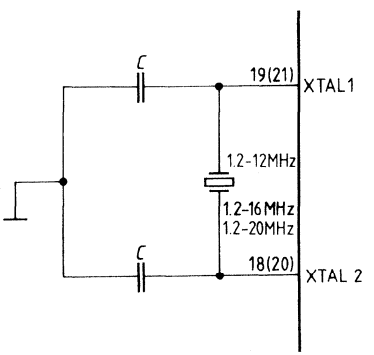
Data Memory Read Cycle



Data Memory Write Cycle

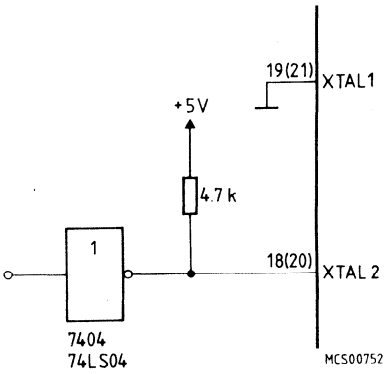


Recommended Oscillator Circuits



$C = 30\ pF \pm 10\ pF$

Crystal Oscillator Mode



Driving from External Source

Pin numbers in (. . .) are specified for PL-CC-44 package.

SIEMENS

8-Bit CMOS Microcontroller — SAB 80C52/80C32

Preliminary

SAB 80C52/80C52-16	CMOS microcontroller with factory-maskprogrammable ROM
SAB 80C32/80C32-16	CMOS microcontroller for external ROM
SAB 80C52-T40/85, **SAB 80C32-T40/85**	extended temperature range: – 40 to + 85 °C (for 12 MHz)
SAB 80C52-T40/110, **SAB 80C32-T40/110**	extended temperature range: – 40 to +110 °C (for 12 MHz)
SAB 80C52-16-T40/85, **SAB 80C32-16-T40/85**	extended temperature range: – 40 to + 85 °C (for 16 MHz)
SAB 80C52-16-T40/110, **SAB 80C32-16-T40/85**	extended temperature range: – 40 to + 110 °C (for 16 MHz)

- 8 K × 8 ROM (SAB 80C52 only)
- 256 K × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- High-performance full-duplex serial channel with flexible transmit/receive baud rate capability
- External memory expandable up to 128 Kbytes
- Versions for 12 MHz and 16 MHz operating frequenzy
- Boolean processor
- Most instructions execute in 1 µs (750 ns)
- Multiply and divide in 4 µs (3 µs)
- Six interrupt sources, two priority levels
- Idle and power-down operation
- P-DIP-40 and PL-CC-44 package
- Full backward compatibility with SAB 80C51/80C31

The SAB 80C52/80C32 is a standalone, high-performance CMOS single-chip microcontroller, designed in Siemens ACMOS technology. It is functionally compatible with the SAB 8052A/8032A devices in MYMOS technology.

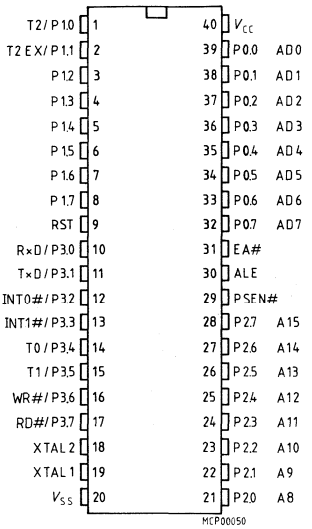
Furthermore, it is backwardly compatible with the SAB 80C51/80C31. The low-power properties of ACMOS technology allow applications where power consumption and dissipation are critical. In addition, the SAB 80C52/80C32 has two software-selectable modes of reduced activity for further power reduction – idle and power-down.

The SAB 80C52 contains a non-volatile 8 K × 8 read-only program memory, a volatile 256 K × 8 read/write data memory, 32 I/O lines, three 16-bit timer/counters, a six-source, two-priority-level interrupt structure, a serial I/O port, an on-chip oscillator, and clock circuits. The SAB 80C32 is identical, except that it lacks the program memory on the chip.

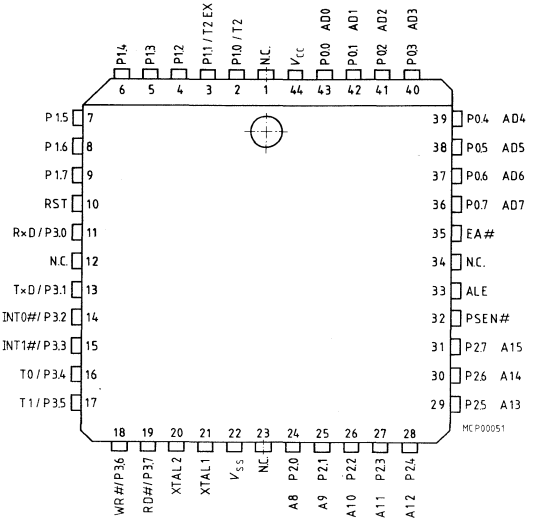
The part is available in a 12 MHz version and in a 16 MHz version which offers an additional performance increase of 33 %. The SAB 80C52/80C32 is supplied in a 40-pin plastic dual-in-line (P-DIP-40) package, or in a 44-pin plastic leaded chip carrier (PL-CC-44) package. The part is available for standard temperature range (0 to 70 °C) and for extended temperature ranges (– 40 to 85 °C; – 40 to 110 °C).

Pin Configuration

P-DIP-40



PL-CC-44



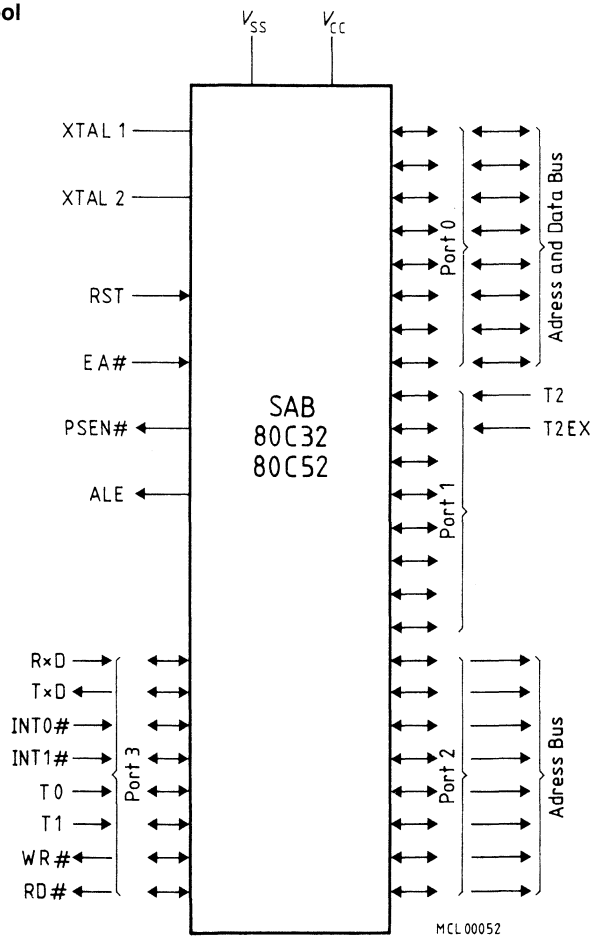
Ordering Information

Type	Ordering code	Package	Description (8-Bit CMOS microcontroller)
SAB 80C52-P	Q67120-C379	P-DIP-40	with factory mask-programmable ROM, 12 MHz
SAB 80C32-P	Q67120-C378	P-DIP-40	for external memory, 12 MHz
SAB 80C52-16-P	Q67120-C501	P-DIP-40	with factory mask-programmable ROM, 16 MHz
SAB 80C32-16-P	Q67120-C500	P-DIP-40	for external memory, 16 MHz
SAB 80C52-P-T40/85	Q67120-C521	P-DIP-40	with factory mask-programmable ROM, 12 MHz, ext. temp. – 40 to 85 °C
SAB 80C32-P-T40/85	Q67120-C520	P-DIP-40	for external memory, 12 MHz, ext. temp. – 40 to 85 °C
SAB 80C52-16-P-T40/85	Q67120-C563	P-DIP-40	with factory mask-programmable ROM, 16 MHz, ext. temp. – 40 to 85 °C
SAB 80C32-16-P-T40/85	Q67120-C527	P-DIP-40	for external memory, 16 MHz, ext. temp. – 40 to 85 °C
SAB 80C52-P-T40/110	Q67120-C558	P-DIP-40	with factory mask-programmable ROM, 12 MHz, ext. temp. – 40 to 110 °C
SAB 80C32-P-T40/110	Q67120-C547	P-DIP-40	for external memory, 12 MHz, ext. temp. – 40 to 110 °C
SAB 80C52-N	Q67120-C396	PL-CC-44	with factory mask-programmable ROM, 12 MHz
SAB 80C32-N	Q67120-C395	PL-CC-44	for external memory, 12 MHz
SAB 80C52-16-N	Q67120-C503	PL-CC-44	with factory mask-programmable ROM, 16 MHz
SAB 80C32-16-N	Q67120-C502	PL-CC-44	for external memory, 16 MHz
SAB 80C52-N-T40/85	Q67120-C564	PL-CC-44	with factory mask-programmable ROM, 12 MHz, ext. temp. – 40 to 85 °C
SAB 80C32-N-T40/85	Q67120-C540	PL-CC-44	for external memory, 12 MHz, ext. temp. – 40 to 85 °C
SAB 80C52-16-N-T40/85	Q67120-C528	PL-CC-44	with factory mask-programmable ROM, 16 MHz, ext. temp. – 40 to 85 °C

Ordering Information (cont'd)

Type	Ordering code	Package	Description (8-Bit CMOS microcontroller)
SAB 80C52-N-T40/110	Q67120-C559	PL-CC-44	with factory mask-programmable ROM, 12 MHz, ext. temp. – 40 to 110 °C
SAB 80C32-N-T40/110	Q67120-C548	PL-CC-44	for external memory, 12 MHz, ext. temp. – 40 to 110 °C

Logic Symbol



Pin Definitions and Functions

Symbol	Pin		Input (I) Output (O)	Functions
	P-DIP-40	PL-CC-44		
P1.0-P1.7	1-8	2-9	I/O	**Port 1** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. Port 1 also receives the low-order address bytes during program verification. Port 1 also contains the timer 2 pins as a secondary function. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 1, as follows: – T2 (P1.0). Input to counter 2. – T2 EX (P1.1). Capture/Reload trigger of timer 2.
RST	9	10	I	A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.
P3.0-P3.7	10-17	11, 13-19	I/O	**Port 3** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and RD# and WR# pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: – RxD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TxD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – INT0# (P3.2). Interrupt 0 input or gate control input for counter 0. – INT1# (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – WR# (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – RD# (P3.7). The read control signal enables external data memory to port 0.

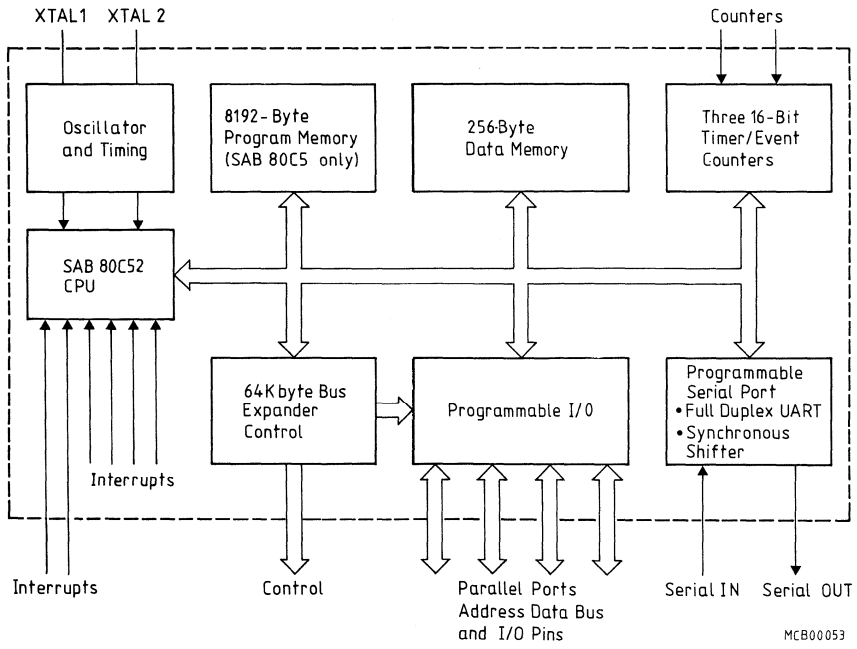
Pin Definitions and Functions (cont'd)

Symbol	Pin		Input (I) Output (O)	Functions
	P-DIP-40	PL-CC-44		
XTAL1 XTAL2	19 18	21 20		**XTAL 1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. **XTAL 2** Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL1 should be driven, while XTAL 2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop. Minimum and maximum high and low times specified in the AC characteristics must be observed.
P2.0-P2.7	21-28	24-31	I/O	**Port 2** is an 8-bit bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resist. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application it uses strong internal pullup resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), port 2 issues the contents of the P2 special function register.
PSEN#	29	32	O	**PROGRAM STORE ENABLE#** This output issues a control signal that enables the external program memory to access the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	33	O	**ADDRESS LATCH ENABLE** Provides signal used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
EA#	31	35	I	**EXTERNAL ACCESS#** When held at a high level, the SAB 80C52 executes instructions from the internal ROM when the PC is less than 8192. When held at a low level, the SAB 80C52 fetches all instructions from the external program memory. For the SAB 80C32 this pin must be tied low.

Pin Definitions and Functions (cont'd)

Symbol	Pin		Input (I) Output (O)	Functions
	P-DIP-40	PL-CC-44		
P0.0-P0.7	39-32	43-36	I/O	**Port 0** is an 8-bit open drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1s. Port 0 also outputs the code bytes during program verification in the SAB 80C52. External pullup resistors are required during program verification.
V_{CC}	40	44		**Supply voltage** during normal, idle, and power-down operations.
V_{SS}	20	22		**Circuit ground potential**.
NC	–	1, 12, 23, 34	–	**No connection**.

Block Diagram



Functional Description

The SAB 80C52/80C32 is functionally compatible with the SAB 8052A/8032A products that are designed in Siemens MYMOS technology. Furthermore, the SAB 80C52/80C32 is backwardly compatible with the SAB 80C51/80C31 devices.

In addition, instead of the RAM backup power supply of the SAB 8052A/8032A, the SAB 80C52/ 80C32 offers two additional power control modes, the idle mode and the power-down mode. The control bits for the reduced power modes are in the special function register PCON.

- Idle mode
  In the idle mode, the CPU puts itself to sleep while all the on-chip peripherals stay active. The instruction that invokes the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The contents of the CPU, the on-chip RAM, and all the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt, at which time the process is picked up at the interrupt service routine and continued, or by a hardware reset which starts the processor in the same way as a power-on reset.
- Power-down mode
  In the power-down mode the oscillator is stopped, and the instruction that invokes power-down is the last instruction executed. Only the contents of the on-chip RAM is preserved. A hardware reset is the only way to terminate power-down.

During power-down and idle mode the external pins will have the following status (see table 1):

Table 1
Status of the External Pins during Idle and Power-Down Modes

Mode	Program Memory	ALE	PSEN	Port 0	Port 1	Port 2	Port 3
Idle	Internal	1	1	Data	Data/ Alternate Outputs	Data	Data/ Alternate Outputs
Idle	External	1	1	Float	Data/ Alternate Outputs	Address	Data/ Alternate Outputs
Power-Down	Internal	0	0	Data	Data/Last Output of Alternate Function	Data	Data/Last Output of Alternate Function
Power-Down	External	0	0	Float	Data/Last Output of Alternate Function	Data	Data/Last Output of Alternate Function

Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A@Ri	AND indirect RAM to accumulator	1	1
ANL	A#data	AND immediate data to accumulator	2	1
ANL	direct, A	AND accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct, A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct, A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate accumulator right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct*)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct, A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1

*) MOV A,ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Notes on data addressing modes:

Rn – Working register R0 – R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is + 127/– 128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7

Hex code	Number of bytes	Mnemonic	Operands
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A, *#data*
25	2	ADD	A, *data addr*
26	1	ADD	A, @R0
27	1	ADD	A, @R1
28	1	ADD	A, R0
29	1	ADD	A, R1
2A	1	ADD	A, R2
2B	1	ADD	A, R3
2C	1	ADD	A, R4
2D	1	ADD	A, R5
2E	1	ADD	A, R6
2F	1	ADD	A, R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A, *#data*
35	2	ADDC	A, *data addr*
36	1	ADDC	A, @R0
37	1	ADDC	A, @R1
38	1	ADDC	A, R0
39	1	ADDC	A, R1
3A	1	ADDC	A, R2
3B	1	ADDC	A, R3
3C	1	ADDC	A, R4
3D	1	ADDC	A, R5
3E	1	ADDC	A, R6
3F	1	ADDC	A, R7

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*, A
43	3	ORL	*data addr, #data*
44	2	ORL	A, *#data*
45	2	ORL	A, *data addr*
46	1	ORL	A, @R0
47	1	ORL	A, @R1
48	1	ORL	A, R0
49	1	ORL	A, R1
4A	1	ORL	A, R2
4B	1	ORL	A, R3
4C	1	ORL	A, R4
4D	1	ORL	A, R5
4E	1	ORL	A, R6
4F	1	ORL	A, R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*, A
53	3	ANL	*data addr, #data*
54	2	ANL	A, *#data*
55	2	ANL	A, *data addr*
56	1	ANL	A, @R0
57	1	ANL	A, @R1
58	1	ANL	A, R0
59	1	ANL	A, R1
5A	1	ANL	A, R2
5B	1	ANL	A, R3
5C	1	ANL	A, R4
5D	1	ANL	A, R5
5E	1	ANL	A, R6
5F	1	ANL	A, R7

Hex code	Number of bytes	Mnemonic	Operands
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*, A
63	3	XRL	*data addr, #data*
64	2	XRL	A, *#data*
65	2	XRL	A, *data addr*
66	1	XRL	A, @R0
67	1	XRL	A, @R1
68	1	XRL	A, R0
69	1	XRL	A, R1
6A	1	XRL	A, R2
6B	1	XRL	A, R3
6C	1	XRL	A, R4
6D	1	XRL	A, R5
6E	1	XRL	A, R6
6F	1	XRL	A, R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C, *bit addr*
73	1	JMP	@A + DPTR
74	2	MOV	A, *#data*
75	3	MOV	data addr, #data
76	2	MOV	@R0, *#data*
77	2	MOV	@R1, *#data*
78	2	MOV	R0, *#data*
79	2	MOV	R1, *#data*
7A	2	MOV	R2, *#data*
7B	2	MOV	R3, *#data*
7C	2	MOV	R4, *#data*
7D	2	MOV	R5, *#data*
7E	2	MOV	R6, *#data*
7F	2	MOV	R7, *#data*

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C, *bit addr*
83	1	MOVC	A, @A + PC
84	1	DIV	AB
85	3	MOV	*data addr, data addr*
86	2	MOV	*data addr,* @R0
87	2	MOV	*data addr,* @R1
88	2	MOV	data addr, R0
89	2	MOV	*data addr,* R1
8A	2	MOV	*data addr,* R2
8B	2	MOV	*data addr,* R3
8C	2	MOV	*data addr,* R4
8D	2	MOV	*data addr,* R5
8E	2	MOV	*data addr,* R6
8F	2	MOV	*data addr,* R7
90	3	MOV	DPTR, *#data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr,* C
93	1	MOVC	A, @A + DPTR
94	2	SUBB	A, *#data*
95	2	SUBB	A, *data addr*
96	1	SUBB	A, @R0
97	1	SUBB	A, @R1
98	1	SUBB	A, R0
99	1	SUBB	A, R1
9A	1	SUBB	A, R2
9B	1	SUBB	A, R3
9C	1	SUBB	A, R4
9D	1	SUBB	A, R5
9E	1	SUBB	A, R6
9F	1	SUBB	A, R7

Hex code	Number of bytes	Mnemonic	Operands
A0	2	ORL	C, */bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C, *bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0, *data addr*
A7	2	MOV	@R1, *data addr*
A8	2	MOV	R0, *data addr*
A9	2	MOV	R1, *data addr*
AA	2	MOV	R2, *data addr*
AB	2	MOV	R3, *data addr*
AC	2	MOV	R4, *data addr*
AD	2	MOV	R5, *data addr*
AE	2	MOV	R6, *data addr*
AF	2	MOV	R7, *data addr*
B0	2	ANL	C, */bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A, *#data, code addr*
B5	3	CJNE	A, *data addr, code addr*
B6	3	CJNE	@R0,*#data, code addr*
B7	3	CJNE	@R1,*#data, code addr*
B8	3	CJNE	R0, *#data, code addr*
B9	3	CJNE	R1, *#data, code addr*
BA	3	CJNE	R2, *#data, code addr*
BB	3	CJNE	R3, *#data, code addr*
BC	3	CJNE	R4, *#data, code addr*
BD	3	CJNE	R5, *#data, code addr*
BE	3	CJNE	R6, *#data, code addr*
BF	3	CJNE	R7, *#data, code addr*

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex code	Number of bytes	Mnemonic	Operands
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A, *data addr*
C6	1	XCH	A, @R0
C7	1	XCH	A, @R1
C8	1	XCH	A, R0
C9	1	XCH	A, R1
CA	1	XCH	A, R2
CB	1	XCH	A, R3
CC	1	XCH	A, R4
CD	1	XCH	A, R5
CE	1	XCH	A, R6
CF	1	XCH	A, R7
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr, code addr*
D6	1	XCHD	A, @R0
D7	1	XCHD	A, @R1
D8	2	DJNZ	R0, *code addr*
D9	2	DJNZ	R1, *code addr*
DB	2	DJNZ	R3, *code addr*
DC	2	DJNZ	R4, *code addr*
DD	2	DJNZ	R5, *code addr*
DE	2	DJNZ	R6, *code addr*
DF	2	DJNZ	R7, *code addr*
E0	1	MOVX	A, @DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A, @R0
E3	1	MOVX	A, @R1
E4	1	CLR	A
E5	2	MOV	A, *data addr* *)
E6	1	MOV	A, @R0
E7	1	MOV	A, @R1
E8	1	MOV	A, R0
E9	1	MOV	A, R1
EA	1	MOV	A, R2
EB	1	MOV	A, R3
EC	1	MOV	A, R4
ED	1	MOV	A, R5
EE	1	MOV	A, R6
EF	1	MOV	A, R7
F0	1	MOVX	@DPTR, A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0, A
F3	1	MOVX	@R1, A
F4	1	CPL	A
F5	2	MOV	*data addr*, A
F6	1	MOV	@R0, A
F7	1	MOV	@R1, A
F8	1	MOV	R0, A
F9	1	MOV	R1, A
FA	1	MOV	R2, A
FB	1	MOV	R3, A
FC	1	MOV	R4, A
FD	1	MOV	R5, A
FE	1	MOV	R6, A
FF	1	MOV	R7, A

*) MOV A, ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias ..... 0 to + 70 °C (SAB 80C52/80C32)
– 40 to + 85 °C (SAB 80C52/80C32-T40/85)
– 40 to + 110 °C (SAB 80C52/80C32-T40/110)
Storage temperature ..... – 65 to + 150 °C
Voltage on any pin with respect to ground (V_{SS}) .....– 0.5 to V_{CC} + 0.5 V
Voltage on V_{CC} to V_{SS} .....– 0.5 to + 6.5 V
Power dissipation..... 1 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V; T_A = 0 to 70 °C (SAB 80C52/80C32)
T_A = – 40 to + 85 °C (SAB 80C52/80C32-T40/85)
T_A = – 40 to + 110 °C (SAB 80C52/80C32-T40/110)

Symbol	Parameter	Limit Values		Unit	Test Condition
		min.	max.		
V_{IL}	Input low voltage (except EA)				–
	for SAB 80C52/80C32, 80C52/80C32-T40/85	– 0.5	0.2 V_{CC} – 0.1	V	
	for SAB 80C52/80C32, T40/110	– 0.5	0.2 V_{CC} – 0.3	V	
V_{IL1}	Input low voltage (EA)	– 0.5	0.2 V_{CC} – 0.3	V	–
V_{IH}	Input high voltage (except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
V_{IH1}	Input high voltage (XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V	–
V_{OL}	Output low voltage (ports 1, 2, 3)	–	0.45	V	I_{OL} = 1.6 mA [1]
V_{OL1}	Output low voltage (port 0, ALE, PSEN)	–	0.45	V	I_{OL} = 3.2 mA [1]
V_{OH}	Output high voltage (ports 1, 2, 3)	2.4 0.9 V_{CC}	– –	V V	I_{OH} = – 80 µA I_{OH} = – 10 µA
V_{OH1}	Output high voltage (port 0 in external bus mode, ALE, PSEN)	2.4 0.9 V_{CC}	– –	V V	I_{OH} = – 800 µA I_{OH} = – 80 µA [2]
I_{IL}	Logical 0 input current (ports 1, 2, 3)	–	– 50	µA	V_{IN} = 0.45 V
I_{TL}	Logical 1-to-0 transition current (ports 1, 2, 3)	–	– 650	µA	V_{IN} = 2 V

Notes see page 490.

DC Characteristics (cont'd)

Symbol	Parameter	Limit Values		Unit	Test Condition
		min.	max.		
I_{LI}	Input leakage current (port 0, EA)	–	± 10	µA	$0.45 < V_{IN} < V_{CC}$
R_{RST}	Reset pulldown resistor	40	150	kΩ	–
C_{IO}	Pin capacitance	–	10	pF	f_c = 1 MHz, T_A = 25 °C
	Power supply current:				
I_{CC}	Active mode, 12 MHz [6]	–	20	mA	V_{CC} = 5 V [4]
I_{CC}	Active mode, 16 MHz [6]	–	26	mA	V_{CC} = 5 V [4]
I_{CC}	Idle mode,12 MHz [6]	–	6.8	mA	V_{CC} = 5 V [5]
I_{CC}	Idle mode,16 MHz [6]	–	8.4	mA	V_{CC} = 5 V [5]
I_{PD}	Power Down Mode	–	50	µA	V_{CC} = 2...5.5 V [3]

Notes see page 418.

Notes for pages 416 and 417 :

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a Schmitt-trigger, or use an address latch with a Schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.

3) Power-down I_{CC} is measured with: EA = Port 0 = V_{CC}; XTAL1 = V_{SS}; XTAL2 = N.C.; RST = V_{SS}; all other pins are disconnected.

4) I_{CC} (active mode) is measured with: XTAL1 driven with clock signal according to the figure below; XTAL2 = N.C.; EA# = Port 0 = V_{CC}; RST = V_{CC}; all other pins are disconnected. I_{CC} might be slightly higher if a crystal oscillator is used.

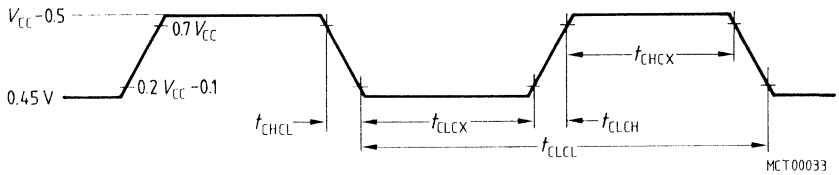
5) I_{CC} (idle mode) is measured with: XTAL1 driven with clock signal according to the figure below; XTAL2 = N.C.; EA# = V_{SS}; Port 0 = V_{CC}; RST = V_{SS}; all other pins are disconnected.

6) $I_{CC\ Max}$ at other frequencies is given by:

active mode: $I_{CC\ Max} = 1.5 * f_{OSC} + 2.0$
idle mode: $I_{CC\ Max} = 0.4 * f_{OSC} + 2.0$

where f_{OSC} is the oscillator frequency im MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V (see also notes 5 and 6)

Clock Signal Waveform for I_{CC} Tests in Active and Idle Mode



AC Characteristics for SAB 80C52/80C32

V_{CC} = 5 V ± 10%; V_{SS} = 0 V; T_A = 0 to 70 °C; (SAB 80C52/80C32)
T_A = – 40 to + 85 °C; (SAB 80C52/80C32 – T40/85)
T_A = – 40 to + 110 °C; (SAB 80C52/80C32 – T40/110)

(C_L for port 0, ALE and PSEN# outputs = 100 pF; C_L for all other outputs = 80 pF)

Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 to 12 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}$– 40	–	ns
t_{AVLL}	Address setup to ALE	53	–	t_{CLCL}– 30	–	ns
t_{LLAX1}	Address hold after ALE	48	–	t_{CLCL}– 35	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	$4t_{CLCL}$– 100	ns
t_{LLPL}	ALE to PSEN#	58	–	t_{CLCL}– 25	–	ns
t_{PLPH}	PSEN# pulse width	215	–	$3t_{CLCL}$– 35	–	ns
t_{PLIV}	PSEN# to valid instruction in	–	150	–	$3t_{CLCL}$– 100	ns
t_{PXIX}	Input instruction hold after PSEN	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float after PSEN#	–	63	–	t_{CLCL}– 20	ns
t_{PXAV}*)	Address valid after PSEN#	75	–	t_{CLCL}– 8	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	$5t_{CLCL}$– 115	ns
t_{PLAZ}	Address float to PSEN#	–	0	–	0	ns

*) Interfacing the SAB 80C52/80C32 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 to 12 MHz		
		min.	max.	min.	max.	

External Data Memory Characteristics

t_{RLRH}	RD# pulse width	400	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	WR# pulse width	400	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	132	–	$2t_{CLCL}-35$	–	ns
t_{RLDV}	RD# to valid data in	–	252	–	$5t_{CLCL}-165$	ns
t_{RHDX}	Data hold after RD#	0	–	0	–	ns
t_{RHDZ}	Data float after RD#	–	97	–	$2t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	517	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	585	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to WR# or RD#	200	300	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address valid to WR# or RD#	203	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	WR# or RD# high to ALE high	43	123	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{QVWX}	Data valid to WR# transition	33	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before WR#	433	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after WR#	33	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after RD#	–	0	–	0	ns

External Clock Drive XTAL1

Symbol	Parameter	Limit Values		Unit
		Variable clock Frequ. = 0.5 to 12 MHz		
		min.	max.	
t_{CLCL}	Oscillator period	83.3	2000	ns
t_{CHCX}	High time	20	$t_{CLCL}-t_{CLCX}$	ns
t_{CLCX}	Low time	20	$t_{CLCL}-t_{CHCX}$	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

AC Characteristics for SAB 80C52-16/80C32-16

V_{CC} = 5 V ± 10%; V_{SS} = 0 V; T_A = 0 to + 70 °C (SAB 80C52/80C32)
T_A = – 40 to + 85 °C (SAB 80C52/80C32 – T40/85)

(C_L for port 0, ALE and PSEN# outputs = 100 pF; C_L for all other outputs = 80 pF)

Symbol	Parameter	Limit Values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 to 16 MHz		
		min.	max.	min.	max.	

Program Memory Characteristics

t_{LHLL}	ALE pulse width	85	–	$2t_{CLCL}$– 40	–	ns
t_{AVLL}	Address setup to ALE	33	–	t_{CLCL}– 30	–	ns
t_{LLAX1}	Address hold after ALE	28	–	t_{CLCL}– 35	–	ns
t_{LLIV}	ALE low to valid instruction in	–	150	–	$4t_{CLCL}$– 100	ns
t_{LLPL}	ALE to PSEN#	38	–	t_{CLCL}– 25	–	ns
t_{PLPH}	PSEN# pulse width	153	–	$3t_{CLCL}$– 35	–	ns
t_{PLIV}	PSEN# to valid instruction in	–	88	–	$3t_{CLCL}$– 100	ns
t_{PXIX}	Input instruction hold after PSEN	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float after PSEN#	–	48	–	t_{CLCL}– 15	ns
t_{PXAV}*)	Address valid after PSEN#	60	–	t_{CLCL}–3	–	ns
t_{AVIV}	Address to valid instruction in	–	223	–	$5t_{CLCL}$– 90	ns
t_{PLAZ}	Address float to PSEN#	0	–	0	–	ns

*) Interfacing the SAB 80C52/80C32-16 to devices with float times up to 55 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

Symbol	Parameter	Limit Values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 0.5 to 16 MHz		
		min.	max.	min.	max.	

External Data Memory Characteristics

t_{RLRH}	RD# pulse width	275	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	WR# pulse width	275	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	90	–	$2t_{CLCL}-35$	–	ns
t_{RLDV}	RD# to valid data in	–	148	–	$5t_{CLCL}-165$	ns
t_{RHDX}	Data hold after RD#	0	–	0	–	ns
t_{RHDZ}	Data float after RD#	–	55	–	$2t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	350	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	398	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to WR# or RD#	138	238	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address valid to WR# or RD#	120	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	WR# or RD# high to ALE high	23	103	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{QVWX}	Data valid to WR# transition	13	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before WR#	288	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after WR#	13	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after RD#	–	0	–	0	ns

External Clock Drive XTAL1

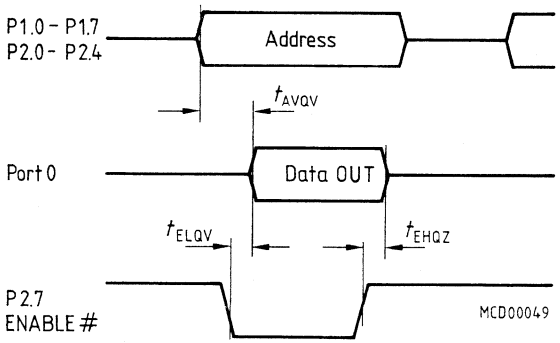
Symbol	Parameter	Limit Values		Unit
		Variable clock Frequ. = 0.5 to 16 MHz		
		min.	max.	
t_{CLCL}	Oscillator period	62.5	2000	ns
t_{CHCX}	High time	15	$t_{CLCL}-t_{CLCX}$	ns
t_{CLCX}	Low time	15	$t_{CLCL}-t_{CHCX}$	ns
t_{CLCH}	Rise time	–	15	ns
t_{CHCL}	Fall time	–	15	ns

ROM Verification Characteristics for SAB 80C52

T_A = 25 °C ± 5 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	48 t_{CLCL}	ns
ENABLE# to valid data	t_{ELQV}	–	48 t_{CLCL}	ns
Data float after ENABLE#	t_{EHQZ}	0	48 t_{CLCL}	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz

ROM Verification



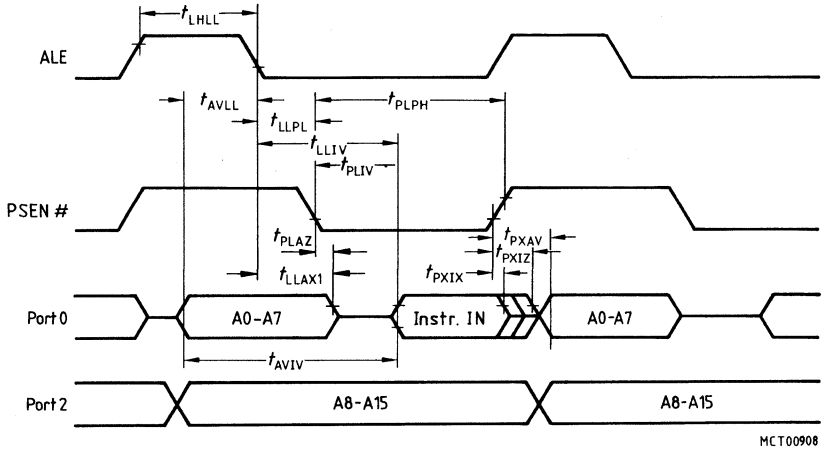
Address: P1.0–P1.7 = A0–A7
P2.0–P2.4 = A8–A12

Data: Port 0 = D0–D7

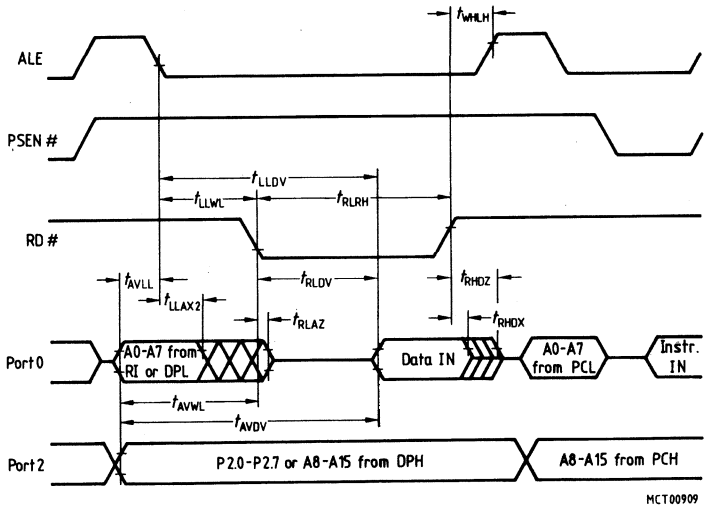
Inputs: P2.5–P2.6, PSEN# = V_{SS}
ALE, EA# = V_{IH}
RST = V_{IH1}

Waveforms

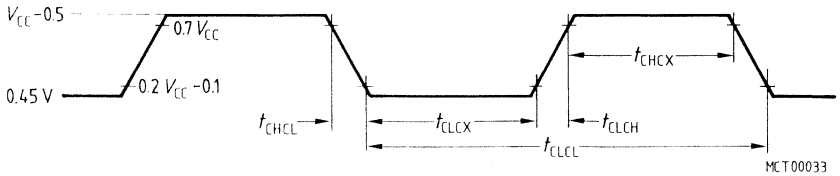
Program Memory Read Cycle



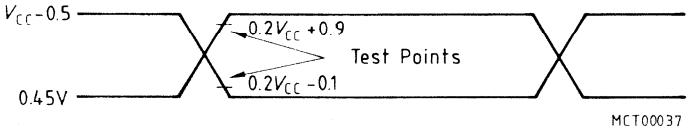
Data Memory Read Cycle



External Clock Cycle

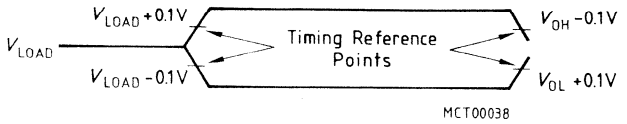


AC Testing: Input, Output Waveforms



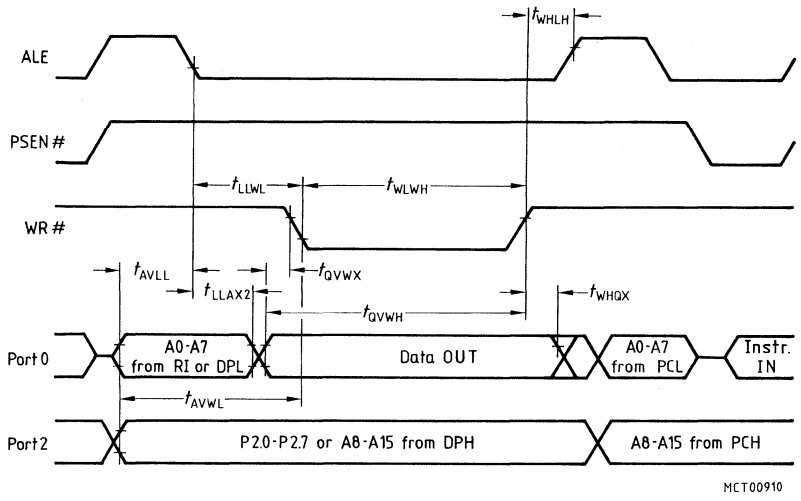
AC Inputs during testing are driven at V_{CC}-0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at $V_{IH\ min}$ for a logic '1' and $V_{IL\ max}$ for a logic '0'

AC Testing: Float Waveforms

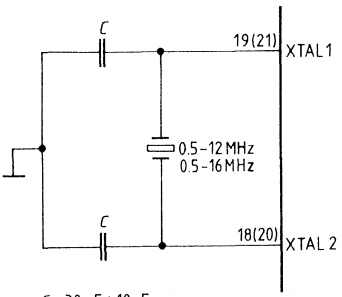


For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OH}/I_{OH} \geq \pm$ 20 mA.

Data Memory Write Cycle

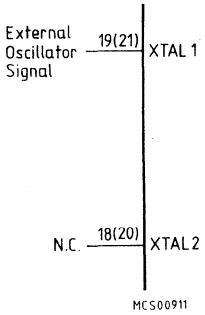


Recommended Oscillator Circuits



$C = 30\,pF \pm 10pF$

Crystal Oscillator Mode



Driving from External Source

Pin numbers in (. . .) are for PL-CC-44 package

SIEMENS

8-Bit Single Chip Microcontroller — SAB 83515-4

Preliminary Data

SAB 83515-4 **Microcontroller with factory mask-programmable ROM**
SAB 83515-4-T3 **ext. temperature range: – 40 to 85 °C**
SAB 83515-4-T4 **ext. temperature range: – 40 to 110 °C**

- 16 K × 8 ROM
- 256 × 8 RAM
- Six 8-bit I/O ports, one 8-bit input port for analog signals
- Three 16-bit timer/counters
- Highly flexible reload, capture, compare capabilities
- Full-duplex serial channel
- Twelve interrupt vectors, four priority levels
- 8-bit A/D converter with 8 multiplexed inputs and programmable internal reference voltages
- 16-bit watchdog timer
- V_{PD} provides standby current for 40 bytes of RAM
- Boolean processor
- 256 bit-addressable locations
- Most instructions execute in 1 µs
- 4 µs multiply and divide
- External memory expandable up to 128 Kbyte
- Backward compatible with SAB 8051
- Three temperature ranges available:
  - SAB 83515-4: 0 to 70 °C
  - SAB 83515-4-T3: – 40 to 85 °C
  - SAB 83515-4-T4: – 40 to 110 °C
- 68-pin plastic leaded chip carrier package (PL-CC-68)

The SAB 83515-4 is a powerful member of the Siemens SAB 8051 family of 8-bit microcontrollers. It is fabricated in + 5 V N-channel, silicon-gate Siemens MYMOS technology.

The SAB 83515-4 is a stand-alone, high-performance single-chip microcontroller based on the SAB 8051 architecture. While maintaining all the SAB 8051 operating characteristics, the SAB 83515-4 incorporates several enhancements which significantly increase design flexibility and overall system performance.

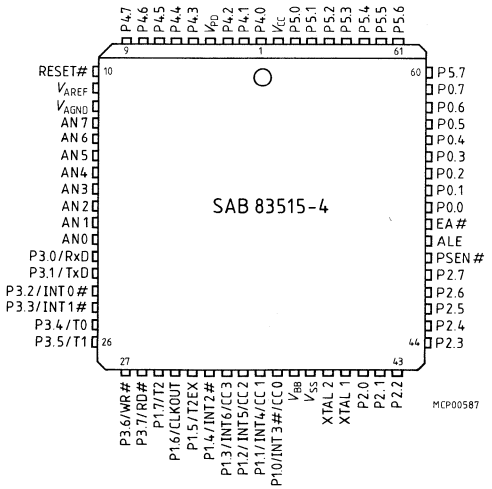
The SAB 83515-4 is functionally compatible with the SAB 80515 with exception of the greater ROM size.

The SAB 83515-4 is supplied in a 68-pin plastic leaded chip carrier package (PL-CC-68).

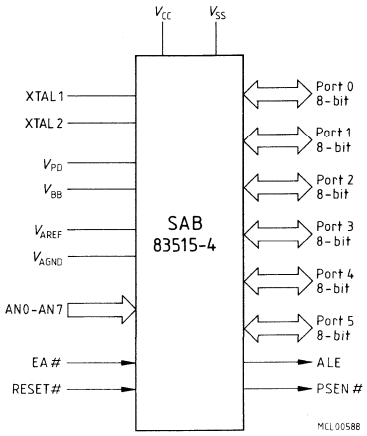
Ordering Information

Type	Ordering code	Package	Function
SAB 83515-4-N	Q67120-C525	PL-CC-68	8-Bit single-chip microcontroller with 16 KByte mask-programmable ROM
SAB 83515-4-N-T3	Q67120-C536	PL-CC-68	like SAB 83515-4, but with ext. temperature range
SAB 83515-4-N-T4	Q67120-C539	PL-CC-68	like SAB 83515-4, but with ext. temperature range

Pin Configuration
(PL-CC-68)



Logic Symbol



Pin Definitions and Functions

Symbol	Pin Number	Input (I) Output (O)	Function
P4.0-P4.7	1-3, 5-9	I/O	**Port 4** is an 8-bit quasi-bidirectional I/O port. Port 4 can sink/source 4 LS-TTL loads.
V_{PD}	4		**Power Down Supply**. If V_{PD} is held within its specs while V_{CC} drops below specs, V_{PD} will provide standby power to 40 bytes of the internal RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
RESET#	10	I	A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 83515-4. A small internal pull-up resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	11		**Reference voltage** for the A/D converter
V_{AGND}	12		**Reference ground** for the A/D converter
AN7-AN0	13-20	I	**Multiplexed analog inputs**
P3.0-P3.7	21-28	I/O	**Port 3** is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source 4 LS-TTL lods. The secondary functions are assigned to the pins of port 3, as follows: – R×D (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) – T×D (P3.1): serial port's transmitter data output(asynchronous) or clock output (synchronous) – INT0# (P3.2): interrupt 0 input / timer 0 gate control input – INT1# (P3.3): interrupt 1 input / timer 1 gate control input – T0 (P3.4): counter 0 input – T1 (P3.5): counter 1 input – WR# (P3.6): the write control signal latches the data byte from port 0 into the external data memory – RD# (P3.7): the read control signal enables the external data memory to port 0

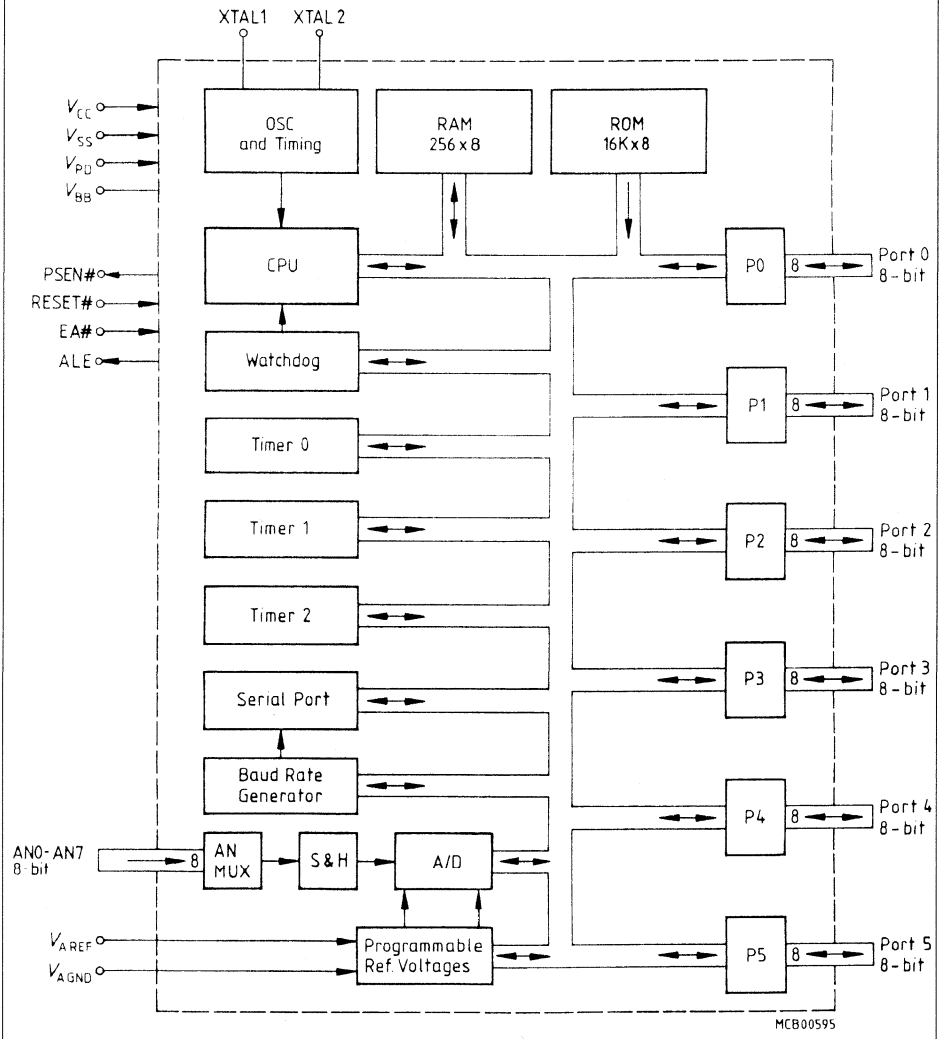
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Input (I) Output (O)	Function
P1.7-P1.0	29-36	I/O	**Port 1** is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. It also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch must be programmed to a one (1) for that function to operate (except when used for the compare functions). Port 1 can sink/source 4 LS-TTL loads. The secondary functions are assigned to the pins of port 3, as follows: – INT3#/CC0 (P1.0): interrupt 3 input / compare 0 output / capture 0 input – INT4/CC1 (P1.1): interrupt 4 input / compare 1 output / capture 1 input – INT5/CC2 (P1.2): interrupt 5 input / compare 2 output / capture 2 input – INT6/CC3 (P1.3): interrupt 6 input / compare 3 output / capture 3 input – INT2# (P1.4): interrupt 2 input – T2EX (P1.5): timer 2 external reload trigger input – CLKOUT (P1.6): system clock output – T2 (P1.7): counter 2 input
V_{BB}	37		**Substrate pin**. Must be connected to V_{SS} through a capacitor (47 to 100 NF) for proper operation of the A/D converter.
XTAL2	39		**XTAL2** is the output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal, ceramic resonator, or external source can be used.
XTAL1	40		**XTAL1** is the input to the oscillator's high gain amplifier. Required when a crystal or ceramic resonator is used. Connect to V_{SS} when external source is used on XTAL2.
P2.0	41-48	I/O	**Port 2** is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source 4 LS-TTL loads.
PSEN#	49	O	The **program store enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.

Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Input (I) Output (O)	Function
ALE	50	O	Provides **adress latch enable** output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
EA#	51	I	When held at a TTL high level, the SAB 83515-4 executes instructions from the internal ROM when the PC is less than 4000H. When held at a TTL low level, the SAB 83515-4 fetches all instructions from external program memory.
P0.0-P0.7	52-59	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source 8 LS-TTL loads.
P5.7-P5.0	60-67	I/O	**Port 5** is an 8-bit quasi-bidirectional I/O port. Port 5 can sink/source 4 LS-TTL loads.
V_{CC}	68		**Power Supply**
V_{SS}	38		**Ground** (0 V)

Figure 1
Block Diagram



Functional Description

The members of the SAB 80515 family of microcontrollers are:

- SAB 80515: Microcontroller, designed in Siemens MYMOS technology, with 8 Kbyte factory mask-programmable ROM
- SAB 80535: ROM-less version of the SAB 80515
- SAB 83515-4: Version of the SAB 80515 with 16 Kbyte factory mask-programmable ROM
- SAB 80C515: Microcontroller, designed in Siemens ACMOS technology, with 8 Kbyte factory mask-programmable ROM
- SAB 80C535: ROM-less version of the SAB 80C515
- SAB 80515K: Special ROM-less version of the SAB 80515 with an additional interface for program memory accesses. An external ROM that is accessed via this interface substitutes the SAB 80515's internal ROM.

The SAB 80535 is identical to the SAB 80515, except that it lacks the on-chip ROM.

Principles of Architecture

The architecture of the SAB 83515-4 is based on the SAB 8051 microcontroller family. The following features of the SAB 83515-4 are fully compatible with the SAB 8051 features:

- Instruction set
- External memory expansion interface (port 0 and port 2)
- Full-duplex serial port
- Timer/counter 0 and 1
- Alternate functions on port 3
- The lower 128 bytes of internal RAM and the lower 4 Kbytes of internal ROM

The SAB 83515-4 additionally contains 128 bytes of internal RAM and internal ROM, which results in a total of 256 bytes of RAM and 16 Kbytes of ROM on chip.
The SAB 83515-4 has a new 16-bit timer/counter with a 2:1 prescaler, reload mode, compare and capture capability. It also contains a 16-bit watchdog timer, an 8-bit A/D converter with programmable reference voltages, two additional quasi-bidirectional 8-bit ports, one 8-bit input port for analog signals, and a programmable clock output ($f_{OSC}/12$). Furthermore, the SAB 83515-4 has a powerful interrupt structure with 12 vectors and 4 programmable priority levels.
Figure 1 shows a block diagram of the SAB 83515-4.

CPU

The SAB 83515-4 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15 % three-byte instructions. With a 12 MHz crystal, 58 % of the instructions execute in 1.0 µs.

Memory Organization

The SAB 83515-4 manipulates operands in the four memory address spaces described in the following (Figure 2 illustrates the memory address spaces of the SAB 83515-4).

Program Memory

The SAB 83515-4 has 16 Kbytes of on-chip ROM. The program memory can be externally expanded up to 64 Kbytes. If the EA# pin is held high, the SAB 83515-4 executes out of internal ROM unless the address exceeds 3FFFH. Locations 4000H through 0FFFFH are then fetched from the external program memory. If the EA# pin is held low, the SAB 83515-4 fetches all instructions from the external program memory.

Data memory

The data memory address space consists of an internal and an external memory space. The internal data memory is divided into three physically separate and distinct blocks: the lower 128 bytes of RAM, the upper 128 bytes of RAM, and the 128-byte special function register (SFR) area. While the upper 128 bytes of data memory and the SFR area share the same address locations, they are accessed through different addressing modes. The lower 128 bytes of data memory can be accessed through direct or register-indirect addressing; the upper 128 bytes of RAM can be accessed through register-indirect addressing; the special function registers are accessible through direct addressing. Four 8-register banks, each bank consisting of eight 8-bit multi-purpose registers, occupy locations 0 through 1FH in the lower RAM area. The next 16 bytes, locations 20H through 2FH, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal data memory address space, and the stack depth can be expanded up to 256 bytes.
The external data memory can be expanded up to 64 Kbytes and can be accessed by instructions that use a 16-bit or an 8-bit address.

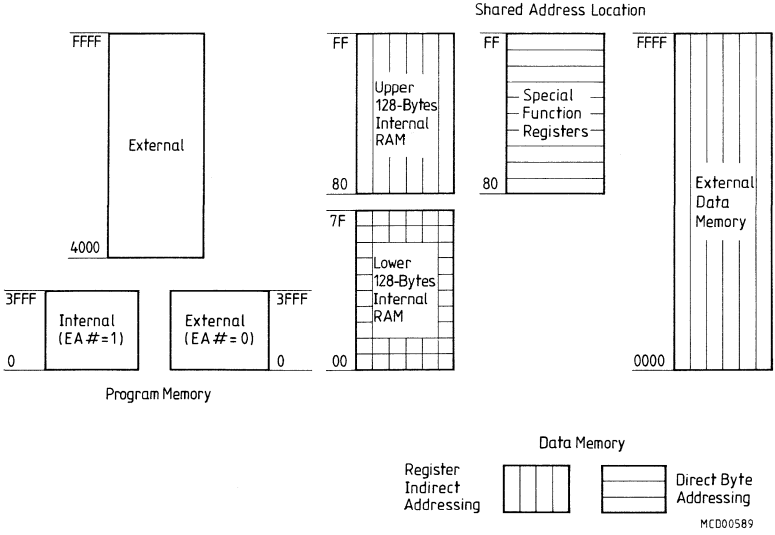
All registers, except the program counter and the four 8-register banks, reside in the special function register area. The 42 special function registers (SFR's) include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripheral functions. There are also 128 directly addressable bits within the SFR area. The special function registers are listed in table 1.

Table 1
Special Function Register

Symbol	Name	Address
* P0	Port 0	80H
SP	Stack pointer	81H
DPL	Data pointer, low byte	82H
DPH	Data pointer, high byte	83H
PCON	Power control register	87H
* TCON	Timer control register	88H
TMOD	Timer mode register	89H
TL0	Timer 0, low byte	8AH
TL1	Timer 1, low byte	8BH
TH0	Timer 0, high byte	8CH
TH1	Timer 1, high byte	8DH
* P1	Port 1	90H
* SCON	Serial port control register	98H
SBUF	Serial port buffer register	99H
* P2	Port 2	0A0H
* IEN0	Interrupt enable register 0	0A8H
IP0	Interrupt priority register 0	0A9H
* P3	Port 3	0B0H
* IEN1	Interrupt enable register 1	0B8H
IP1	Interrupt priority register 1	0B9H
* IRCON	Interrupt request control register	0C0H
CCEN	Compare/capture enable register	0C1H
CCL1	Compare/capture register 1, low byte	0C2H
CCH1	Compare/capture register 1, high byte	0C3H
CCL2	Compare/capture register 2, low byte	0C4H
CCH2	Compare/capture register 2, high byte	0C5H
CCL3	Compare/capture register 3, low byte	0C6H
CCH3	Compare/capture register 3, high byte	0C7H
* T2CON	Timer 2 control register	0C8H
CRCL	Compare/reload/capture register, low byte	0CAH
CRCH	Compare/reload/capture register, high byte	0CBH
TL2	Timer 2, low byte	0CCH
TH2	Timer 2, high byte	0CDH
* PSW	Program status word register	0D0H
* ADCON	A/D converter control register	0D8H
ADDAT	A/D converter data register	0D9H
DAPR	A/D converter program register	0DAH
* ACC	Accumulator	0E0H
* P4	Port 4	0E8H
* B	B register	0F0H
* P5	Port 5	0F8H

The SFR's marked with an asterisk (*) are bit and byte-addressable.

Figure 2
Memory Address Spaces



I/O Ports

The SAB 83515-4 has six 8-bit I/O ports and one 8-bit input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pullup resistors. That means, when configured as inputs, ports 1 to 5 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte and reads/writes the data byte, while port 2 emits the high-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.
Ports 1 and 3 are provided for several alternate functions, as listed below:

Port	Symbol	Function
P1.0	INT3#/CC0	External interrupt 3 input, compare 0 output, capture 0 input
P1.1	INT4/CC1	External interrupt 4 input, compare 1 output, capture 1 input
P1.2	INT5/CC2	External interrupt 5 input, compare 2 output, capture 2 input
P1.3	INT6/CC3	External interrupt 6 input, compare 3 output, capture 3 input
P1.4	INT2#	External interrupt 2 input
P1.5	T2EX	Timer 2 external reload trigger input
P1.6	CLKOUT	System clock output
P1.7	T2	Timer 2 external counter input
P3.0	R × D	Serial port's receiver data input (asynchronous) or data input/output (synchronous)
P3.1	T × D	Serial port's transmitter data output (asynchronous) or clock output (synchronous)
P3.2	INT0#	External interrupt 0 input, timer 0 gate control
P3.3	INT1#	External interrupt 1 input, timer 1 gate control
P3.4	T0	Timer 0 external counter input
P3.5	T1	Timer 1 external counter input
P3.6	WR#	External data memory write strobe
P3.7	RD#	External data memory read strobe

The input port AN0-AN7 is used for analog input signals to the A/D converter.

Timer/Counters

The SAB 83515-4 contains three 16-bit timer/counters which are useful in many applications for timing and counting. The input clock for each timer/counter is 1/12 of the oscillator frequency in the timer operation or can be taken from an external clock source for the counter operation (maximum count rate is 1/24 of the oscillator frequency).

Timer/Counter 0 and 1

These timer/counters can operate in four modes:

Mode 0: 8-bit timer/counter with 32:1 prescaler

Mode 1: 16-bit timer/counter

Mode 2: 8-bit timer/counter with 8-bit auto-reload

Mode 3: Timer/counter 0 is configured as one 8-bit timer/counter and one 8-bit timer; Timer/counter 1 in this mode holds its count.

External inputs INT0# and INT1# can be programmed to function as a gate for timer/counters 0 and 1 to facilitate pulse width measurements.

Timer/Counter 2

Timer/counter 2 of the SAB 83515-4 is a 16-bit timer/counter with several additional features. It offers a 2:1 prescaler, a selectable gate function, and compare, capture and reload functions. Corresponding to the 16-bit timer register there are four 16-bit capture/compare registers, one of them can be used to perform a 16-bit reload on a timer overflow or external event. Each of these registers corresponds to a pin of port 1 for capture input/compare output.
Figure 3 shows a block diagram of timer/counter 2.

– Reload

A 16-bit reload can be performed with the 16-bit CRC register, which is a concatenation of the 8-bit registers CRCL and CRCH. There are two modes from which to select:

Mode 0: Reload is caused by a timer 2 overflow (auto-reload).

Mode 1: Reload is caused in response to a negative transition at pin T2EX (P1.5), which can also request an interrupt.

– Capture

This feature permits saving the actual timer/counter contents into a selected register upon an external event or a software write operation. Two modes are provided to latch the current 16-bit value in timer 2 registers into a dedicated capture register:

Mode 0: Capture is performed in response to a transition at the corresponding port 1 pins CC0 to CC3.

Mode 1: Write operation into the low-order byte of the dedicated capture register causes the timer 2 contents to be latched into this register.

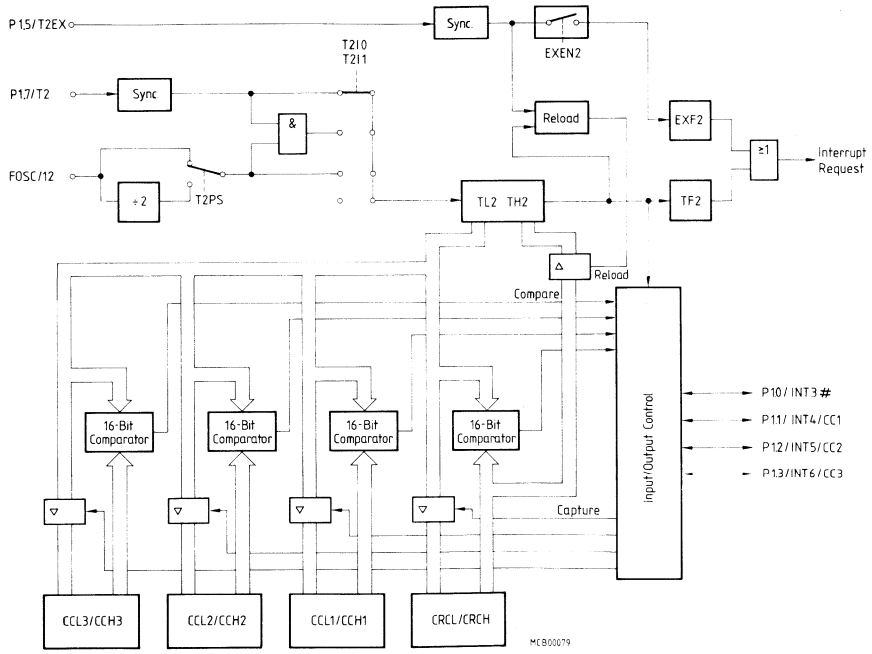
Compare

In the compare mode, the 16-bit values stored in the dedicated compare registers are compared to the contents of the timer 2 registers. If the count value in the timer 2 registers matches one of the stored values, an appropriate output signal is generated and an interrupt is requested. Two compare modes are provided:

Mode 0: Upon a match the output signal charges from low to high. It goes back to a low level when timer 2 overflows.

Mode 1: The transition of the output signal can be determined by software. A timer 2 overflow causes no output change.

Figure 3
Block Diagram of Timer/Counter 2



Serial Port

The serial port of the SAB 83515-4 enables full duplex communication between microcontrollers or between microcontroller and peripheral devices.
The serial port can operate in 4 modes:

Mode 0: Shift register mode. Serial data enters and exits through R × D. T × D outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency.

Mode 1: 10 bits are transmitted (through R × D) or received (through T × D): a start bit (0), 8 data bits (LSB first), and a stop bit (1). The baud rate is variable.

Mode 2: 11 bits are transmitted (through R × D) or received (through T × D): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 11 bits are transmitted (through T × D) or received (through R × D): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Mode 3 is identical to mode 2 except for the baud rate. The baud rate in mode 3 is variable.

The variable baud rates in modes 1 and 3 can be generated by timer 1 or an internal baud rate generator.

A/D Converter

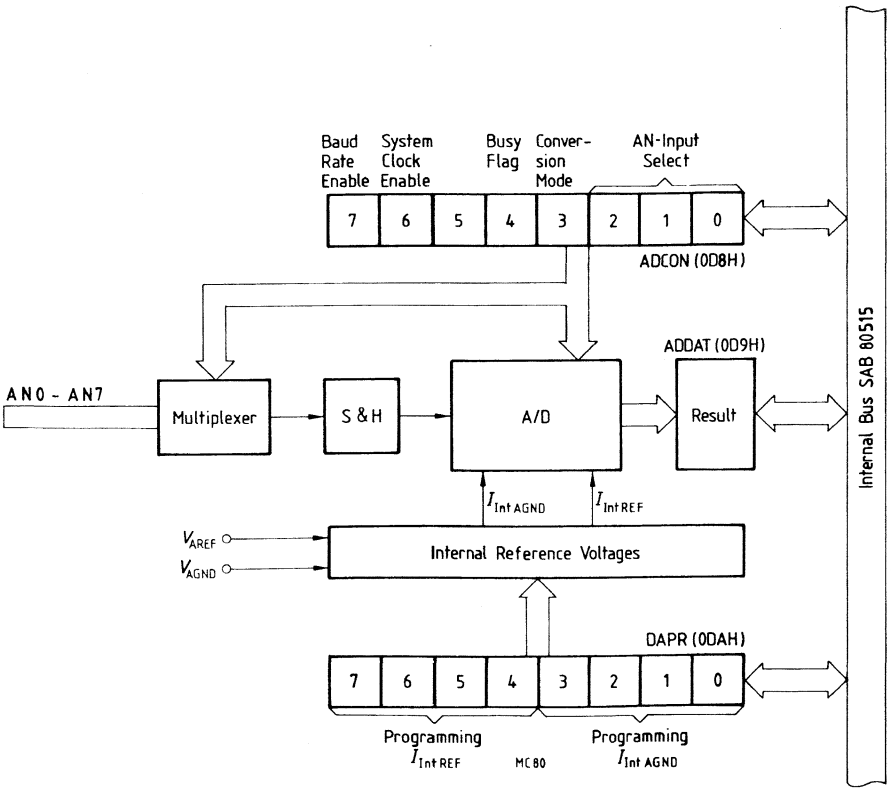
The 8-bit A/D converter of the SAB 83515-4 has eight multiplexed analog inputs and uses the successive approximation method.

Conversion can be programmed to be single or continuous; at the end of a conversion an interrupt can be generated.

A unique feature is the capability of internal reference voltage programming. The internal reference voltages $V_{IntAREF}$ and $V_{IntAGND}$ for the A/D converter both are programmable to one of 16 steps with respect to the external reference voltages. This feature permits a conversion with a smaller internal reference voltage range to gain a higher resolution. In addition, the internal reference voltages can easily be adapted by software to the desired analog input voltage range.

Figure 4 shows a block diagram of the A/D converter.

Figure 4
Block Diagram of the A/D Converter



Interrupt Structure

The SAB 83515-4 has 12 interrupt vectors with the following vector addresses and request flags:

Table 2
Interrupt Sources and Vectors

Source (Request Flags)	Vector	Vector Address
IE0	External interrupt 0	0003H
TF0	Timer 0 interrupt	000BH
IE1	External interrupt 1	0013H
TF1	Timer 1 interrupt	001BH
RI + TI	Serial port interrupt	0023H
TF2 + EXF2	Timer 2 interrupt	002BH
IADC	A/D converter interrupt	0043H
IEX2	External interrupt 2	004BH
IEX3	External interrupt 3	0053H
IEX4	External interrupt 4	005BH
IEX5	External interrupt 5	0063H
IEX6	External interrupt 6	006BH

Each interrupt vector can be individually enabled/disabled. The minimum response time to an interrupt request is more than 3 machine cycles and less than 9 machine cycles.

Figure 5 shows the interrupt request sources.

External interrupts 0 and 1 can be activated by a low-level or a negative transition (selectable) at their corresponding input pin, external interrupts 2 and 3 can be programmed for triggering on a negative or a positive transition. The external interrupts 3 or 6 are combined with the corresponding alternate functions compare (output) and capture (input) on port 1.

For programming of the priority levels the interrupt vectors are combined to pairs. Each pair can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1.

Figure 6 shows the priority level structure.

Figure 5
Interrupt Request Sources

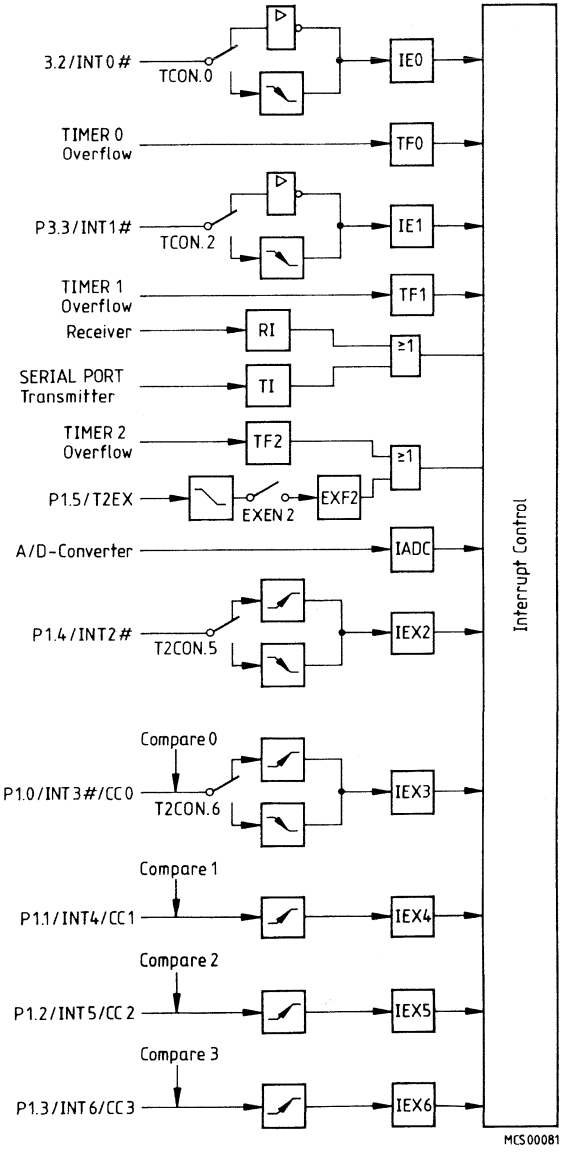
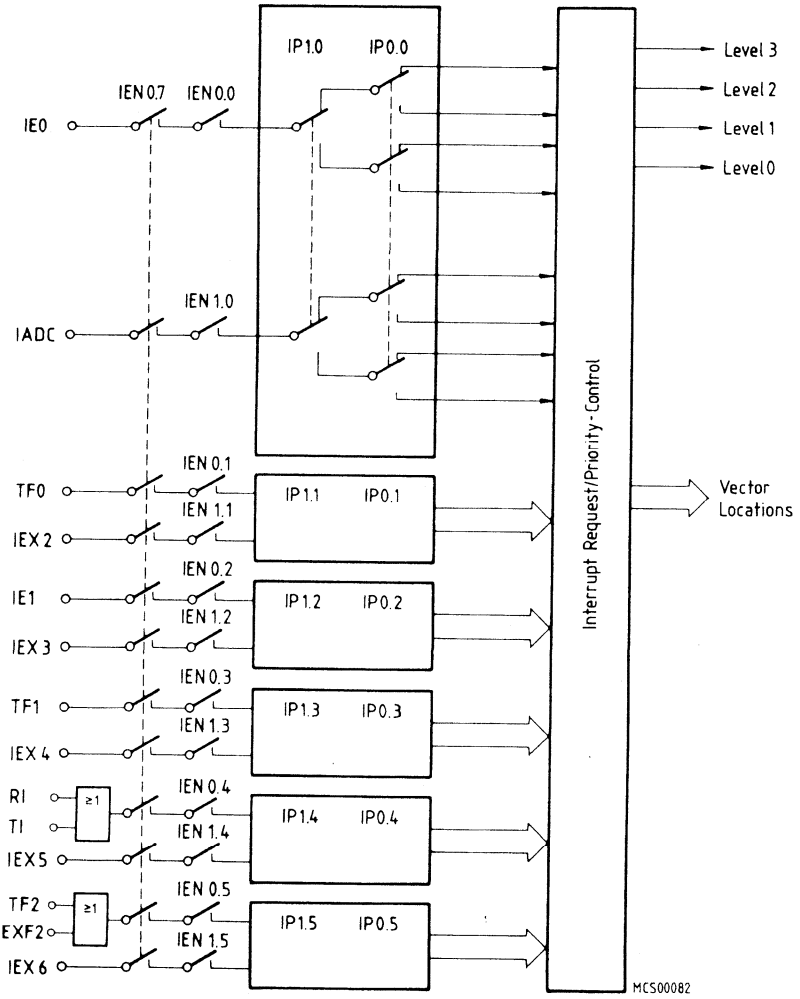


Figure 6
Priority Level Structure



Watchdog Timer

This feature is provided as a means of graceful recovery from a software upset. After an external reset, the watchdog timer is cleared and stopped. It can be started and cleared by software, but it cannot be stopped. If the software fails to clear the watchdog timer at least every 65532 machine cycles (about 65 ms if a 12 MHz oscillator frequency is used), an internal reset will be initiated.

The reset cause (external reset or reset caused by the watchdog) can be examined by software. To clear the watchdog, two bits in two different special function registers must be set by two consecutive instructions (bits IEN0.6 and IEN1.6). This is done to prevent the watchdog from being cleared by unexpected opcodes.

Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct*)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct, A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2
MOV	direct,@R	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A + DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A + PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1

*) MOV A, ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A + DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Notes on data addressing modes:

Rn – Working register R0 – R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is + 127/– 128 bytes relative to first byte of the following instruction.

Instruction Op Codes in Hexadecimal Order

Hex-code	Number of Bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A, *#data*
25	2	ADD	A, *data addr*
26	1	ADD	A, @R0
27	1	ADD	A, @R1
28	1	ADD	A, R0
29	1	ADD	A, R1
2A	1	ADD	A, R2
2B	1	ADD	A, R3
2C	1	ADD	A, R4
2D	1	ADD	A, R5
2E	1	ADD	A, R6
2F	1	ADD	A, R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A, *#data*
35	2	ADDC	A, *data addr*
36	1	ADDC	A, @R0
37	1	ADDC	A, @R1
38	1	ADDC	A, R0
39	1	ADDC	A, R1
3A	1	ADDC	A, R2
3B	1	ADDC	A, R3
3C	1	ADDC	A, R4
3D	1	ADDC	A, R5
3E	1	ADDC	A, R6
3F	1	ADDC	A, R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr, A*
43	3	ORL	*data addr, #data*
44	2	ORL	A, *#data*
45	2	ORL	A, *data addr*
46	1	ORL	A, @R0
47	1	ORL	A, @R1
48	1	ORL	A, R0
49	1	ORL	A, R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex-code	Number of Bytes	Mnemonic	Operands
4A	1	ORL	A, R2
4B	1	ORL	A, R3
4C	1	ORL	A, R4
4D	1	ORL	A, R5
4E	1	ORL	A, R6
4F	1	ORL	A, R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr, A*
53	3	ANL	*data addr, #data*
54	2	ANL	A, *#data*
55	2	ANL	A, *data addr*
56	1	ANL	A, @R0
57	1	ANL	A, @R1
58	1	ANL	A, R0
59	1	ANL	A, R1
5A	1	ANL	A, R2
5B	1	ANL	A, R3
5C	1	ANL	A, R4
5D	1	ANL	A, R5
5E	1	ANL	A, R6
5F	1	ANL	A, R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr, A*
63	3	XRL	*data addr, #data*
64	2	XRL	A, *#data*
65	2	XRL	A, *data addr*
66	1	XRL	A, @R0
67	1	XRL	A, @R1
68	1	XRL	A, R0
69	1	XRL	A, R1
6A	1	XRL	A, R2
6B	1	XRL	A, R3
6C	1	XRL	A, R4
6D	1	XRL	A, R5
6E	1	XRL	A, R6
6F	1	XRL	A, R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C, *bit addr*
73	1	JMP	@A + DPTR
74	2	MOV	A, *#data*
75	3	MOV	*data addr, #data*
76	2	MOV	@R0, *#data*
77	2	MOV	@R1, *#data*
78	2	MOV	R0, *#data*
79	2	MOV	R1, *#data*
7A	2	MOV	R2, *#data*
7B	2	MOV	R3, *#data*
7C	2	MOV	R4, *#data*
7D	2	MOV	R5, *#data*
7E	2	MOV	R6, *#data*
7F	2	MOV	R7, *#data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C, *bit addr*
83	1	MOVC	A, @A + PC
84	1	DIV	AB
85	3	MOV	*data addr, data addr*
86	2	MOV	*data addr,* @R0
87	2	MOV	*data addr*, @R1
88	2	MOV	*data addr*, R0
89	2	MOV	*data addr*, R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*, R4
8D	2	MOV	*data addr*, R5
8E	2	MOV	*data addr*, R6
8F	2	MOV	*data addr*, R7
90	3	MOV	DPTR, *#data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr,* C
93	1	MOVC	A, @A + DPTR

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex-code	Number of Bytes	Mnemonic	Operands
94	2	SUBB	A, *#data*
95	2	SUBB	A, *data addr*
96	1	SUBB	A, @R0
97	1	SUBB	A, @R1
98	1	SUBB	A, R0
99	1	SUBB	A, R1
9A	1	SUBB	A, R2
9B	1	SUBB	A, R3
9C	1	SUBB	A, R4
9D	1	SUBB	A, R5
9E	1	SUBB	A, R6
9F	1	SUBB	A, R7
A0	2	ORL	C, */bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C, *bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0, *data addr*
A7	2	MOV	@R1, *data addr*
A8	2	MOV	R0, *data addr*
A9	2	MOV	R1, *data addr*
AA	2	MOV	R2, *data addr*
AB	2	MOV	R3, *data addr*
AC	2	MOV	R4, *data addr*
AD	2	MOV	R5, *data addr*
AE	2	MOV	R6, *data addr*
AF	2	MOV	R7, *data addr*
B0	2	ANL	C, */bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A, *#data, code addr*
B5	3	CJNE	A,*data addr, code addr*
B6	3	CJNE	@R0, *#data, code addr*
B7	3	CJNE	@R1, *#data, code addr*
B8	3	CJNE	R0, *#data, code addr*
B9	3	CJNE	R1, *#data, code addr*
BA	3	CJNE	R2, *#data, code addr*
BB	3	CJNE	R3, *#data, code addr*
BC	3	CJNE	R4, *#data, code addr*
BD	3	CJNE	R5, *#data, code addr*
BE	3	CJNE	R6, *#data, code addr*
BF	3	CJNE	R7, *#data, code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A, *data addr*
C6	1	XCH	A, @R0
C7	1	XCH	A, @R1
C8	1	XCH	A, R0
C9	1	XCH	A, R1
CA	1	XCH	A, R2
CB	1	XCH	A, R3
CC	1	XCH	A, R4
CD	1	XCH	A, R5
CE	1	XCH	A, R6
CF	1	XCH	A, R7
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr, code addr*
D6	1	XCHD	A, @R0
D7	1	XCHD	A, @R1
D8	2	DJNZ	R0, *code addr*
D9	2	DJNZ	R1, *code addr*
DA	2	DJNZ	R2, *code addr*
DB	2	DJNZ	R3, *code addr*
DC	2	DJNZ	R4, *code addr*
DD	2	DJNZ	R5, *code addr*

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex-code	Number of bytes	Mnemonic	Operands
DE	2	DJNZ	R6, *code addr*
DF	2	DJNZ	R7, *code addr*
E0	1	MOVX	A, @DPTR
E1	2	AJMP	code addr
E2	1	MOVX	A, @R0
E3	1	MOVX	A, @R1
E4	1	CLR	A
E5	2	MOV	A, *data addr* *)
E6	1	MOV	A, @R0
E7	1	MOV	A, @R1
E8	1	MOV	A, R0
E9	1	MOV	A, R1
EA	1	MOV	A, R2
EB	1	MOV	A, R3
EC	1	MOV	A, R4
ED	1	MOV	A, R5
EE	1	MOV	A, R6
EF	1	MOV	A, R7
F0	1	MOVX	@DPTR, A
F1	2	ACALL	code addr
F2	1	MOVX	@R0, A
F3	1	MOVX	@R1, A
F4	1	CPL	A
F5	2	MOV	*data addr*, A
F6	1	MOV	@R0, A
F7	1	MOV	@R1, A
F8	1	MOV	R0, A
F9	1	MOV	R1, A
FA	1	MOV	R2, A
FB	1	MOV	R3, A
FC	1	MOV	R4, A
FD	1	MOV	R5, A
FE	1	MOV	R6, A
FF	1	MOV	R7, A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	0 to + 70 °C (SAB 83515-4)
	– 40 to + 85 °C (SAB 83515-4-T3)
	– 40 to + 110 °C (SAB 83515-4-T4)
Storage temperature	– 65 to + 150 °C
Voltage on any pin with respect to ground (V_{SS})	– 0.5 to + 7 V
Power dissipation	2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V; T_A = 0 to 70 °C for SAB 83515-4
T_A = – 40 to + 85 °C for SAB 83515-4-T3
T_A = – 40 to + 110 °C for SAB 83515-4-T4

Symbol	Parameter	Limit Values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	– 0.5	0.8	V	–
V_{IH}	Input high voltage (except RESET# and XTAL2)	2.0	V_{CC} + 0.5	V	–
V_{IH1}	Input high voltage to XTAL2	2.5	V_{CC} + 0.5	V	XTAL1 to V_{SS}
V_{IH2}	Input high voltage to RESET#	3.0	–	V	
V_{PD}	Power-down voltage	3	5.5	V	V_{CC} = 0 V
V_{OL}	Output low voltage, ports 1, 2, 3, 4, 5	–	0.45	V	I_{OL} = 1.6 mA [1]
V_{OL1}	Output low voltage, port 0, ALE, PSEN#	–	0.45	V	I_{OL} = 3.2 mA [1]
V_{OH}	Output high voltage, ports 1, 2, 3, 4, 5	2.4	–	V	I_{OH} = – 80 µA
V_{OH1}	Output high voltage, port 0, ALE, PSEN#	2.4	–	V	I_{OH} = – 400 µA
I_{IL}	Logic 0 input current, ports 1, 2, 3, 4, 5	–	– 800	µA	V_{IL} = 0.45 V
I_{IL2}	Logic 0 input current, XTAL2	–	– 2.5	mA	XTAL1 = V_{SS} V_{IL} = 0.45 V
I_{IL3}	Input low current to RESET# for reset	–	– 500	µA	V_{IL} = 0.45 V
I_{LI}	Input leakage current to port 0, EA#, AN0-AN7	–	± 1	µA	0 V < V_{IN} < V_{CC}
I_{CC}	Power supply current SAB 83515-4 SAB 83515-4-T3 SAB 83515-4-T4	 – – –	 230 250 250	mA	all outputs disconnected
I_{PD}	Power-down current	–	3	mA	V_{CC} = 0 V
C_{IO}	Capacitance of I/O buffer	–	10	pF	f_C = 1 MHz

1) Capacative loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1, 3, 4, 5. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-0 transitions during bus operation.

A/D Converter Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V; V_{AREF} = V_{CC} ± 5 %; V_{AGND} = V_{SS} ± 0.2 V;
$V_{IntAREF} - V_{IntAGND} \geq 1$ V; T_A = 0 to 70 °C for SAB 83515-4
T_A = – 40 to + 85 °C for SAB 83515-4-T3
T_A = – 40 to + 110 °C for SAB 83515-4-T4

Symbol	Parameter	Limit Values			Unit	Test Condition
		min.	typ.	max.		
V_{AINPUT}	Analog input voltage	V_{AGND} – 0.2	–	V_{AREF} + 0.2	V	–
C_L	Analog input capacitance	–	25	–	pF	1)
t_L	Load time	–	–	2 t_{CY}	µs	–
t_S	Sample time (incl. load time)	–	–	5 t_{CY}	µs	–
t_C	Conversion time (incl. sample time)	–	–	15 t_{CY}	µs	–
DNLE	Differential non-linearity	–	± 1/2	± 1	LSB	$V_{IntAREF}$ =
INLE	Integral non-linearity	–	± 1/2	± 1	LSB	V_{AREF} = V_{CC}
	Offset error		± 1/2	± 1	LSB	$V_{IntAGND}$ =
	Gain error		± 1/2	± 1	LSB	V_{AGND} = V_{SS}
TUE	Total unadjusted error		± 1	± 2	LSB	1)
I_{REF}	V_{AREF} supply current	–	–	5	mA	2)
$V_{IntREFERR}$	Internal reference error	–	± 5	± 15	mV	2)

1) The internal resistance of the analog source must be low enough to assure full loading of the sample capacitance (C_I) during load time (t_L). After charging of the internal capacitance (C_I) in the load time (t_L) the analog input must be held constant for the rest of the sample time (t_S).

2) The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

AC Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V; C_L for port 0, ALE and PSEN# outputs = 100 pF; C_L for all other outputs = 80 pF; T_A = 0 to 70 °C for SAB 83515-4
T_A = – 40 to + 85 °C for SAB 83515-4-T3
T_A = – 40 to + 110 °C for SAB 83515-4-T4

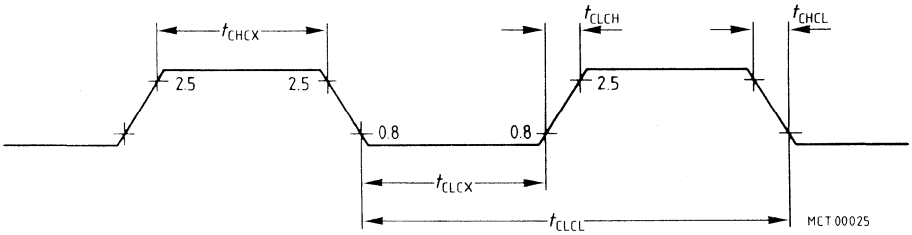
Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 to 12 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
t_{CY}	Cycle time	1000	–	20 t_{CLCL}	–	ns
t_{LHLL}	ALE pulse width	127	–	2 t_{CLCL} – 40	–	ns
t_{AVLL}	Address setup to ALE	53	–	t_{CLCL} – 30	–	ns
t_{LLAX1}	Address hold after ALE	48	–	t_{CLCL} – 35	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	4 t_{CLCL} – 100	ns
t_{LLPL}	ALE to PSEN#	58	–	t_{CLCL} – 25	–	ns
t_{PLPH}	PSEN# pulse width	215	–	3 t_{CLCL} – 35	–	ns
t_{PLIV}	PSEN# to valid instruction in	–	150	–	3 t_{CLCL} – 100	ns
t_{PXIX}	Input instruction hold after PSEN#	0	–	0	–	ns
t_{PXIZ} 1)	Input instruction float after PSEN#	–	63	–	t_{CLCL} – 20	ns
t_{PXAV} 1)	Address valid after PSEN#	75	–	t_{CLCL} – 8	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	5 t_{CLCL} – 115	ns
t_{AZPL}	Address float to PSEN#	0	–	0	–	ns
External Data Memory Characteristics						
t_{RLRH}	RD# pulse width	400	–	6 t_{CLCL} – 100	–	ns
t_{WLWH}	WR# pulse width	400	–	6 t_{CLCL} – 100	–	ns
t_{LLAX2}	Address hold after ALE	132	–	2 t_{CLCL} – 35	–	ns
t_{RLDV}	RD# to valid data in	–	252	–	5 t_{CLCL} – 165	ns
t_{RHDX}	Data hold after RD#	0	–	0	–	ns
t_{RHDZ}	Data float after RD#	–	97	–	2 t_{CLCL} – 70	ns
t_{LLDV}	ALE to valid data in	–	517	–	8 t_{CLCL} – 150	ns
t_{AVDV}	Address to valid data in	–	585	–	9 t_{CLCL} – 165	ns
t_{LLWL}	ALE to WR# or RD#	200	300	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
t_{AVWL}	Address to WR# or RD#	203	–	4 t_{CLCL} – 130	–	ns
t_{WHLH}	WR# or RD# high to ALE high	43	123	t_{CLCL} – 40	t_{CLCL} + 40	ns
t_{QVWX}	Data valid to WR# transition	33	–	t_{CLCL} – 50	–	ns
t_{QVWX}	Data setup before WR#	433	–	7 t_{CLCL} – 150	–	ns
t_{WHQX}	Data hold after WR#	33	–	t_{CLCL} – 50	–	ns
t_{RLAZ}	Address float after RD#	–	0	–	0	ns

1) Interfacing the SAB 83515-4 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

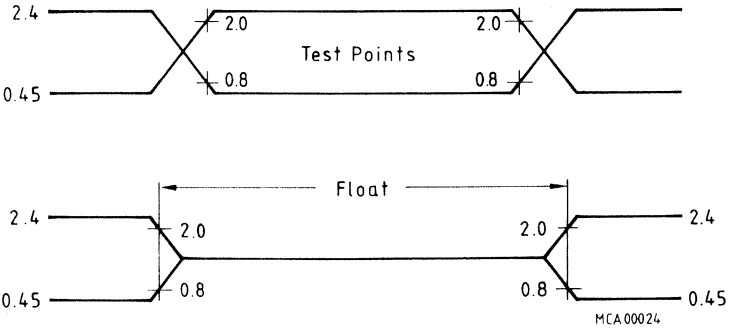
AC Characteristics (cont'd)

Symbol	Parameter	Limit Values		Unit
		Variable clock Freq. = 1.2 to 12 MHz		
		min.	max.	
External Clock Drive XTAL2				
t_{CLCL}	Oscillator period	83.3	833.3	ns
t_{CHCX}	High time	20	$t_{CLCL} - t_{CLCX}$	ns
t_{CLCX}	Low time	20	$t_{CLCL} - t_{CHCX}$	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

External Clock Cycle



AC Testing Input, Output, Float Waveforms

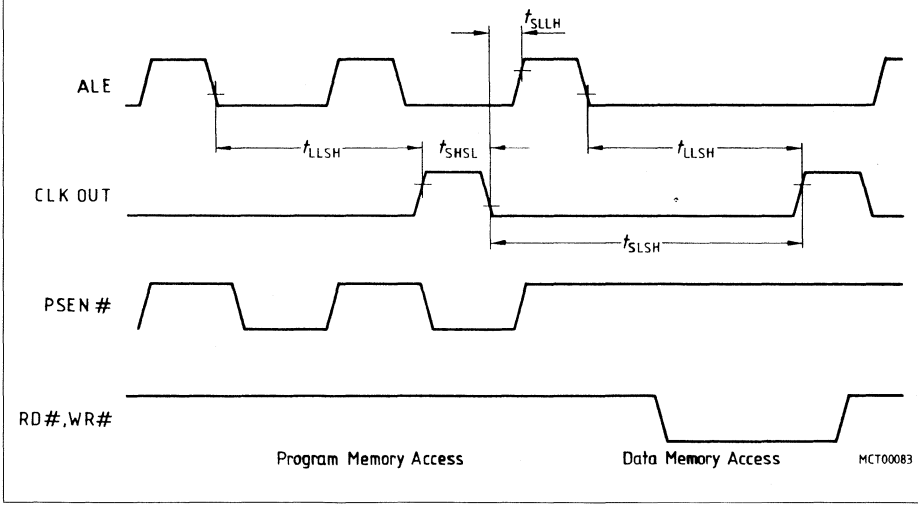


AC testing inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point where a P0 pin sinks 3.2 mA or sources 400 µA at voltage test levels.

AC Characteristics (cont'd)

Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock $1/f_{CLCL}$ = 1.2 to 12 MHz		
		min.	max.	min.	max.	
System Clock Timing						
t_{LLSH}	ALE to CLKOUT	543	–	7 t_{CLCL} – 40	–	ns
t_{SHSL}	CLKOUT high time	127	–	2 t_{CLCL} – 40	–	ns
t_{SLSH}	CLKOUT low time	793	–	10 t_{CLCL} – 40	–	ns
t_{SLLH}	CLKOUT low to ALE high	43	123	t_{CLCL} – 40	t_{CLCL} + 40	ns

System Clock Timing

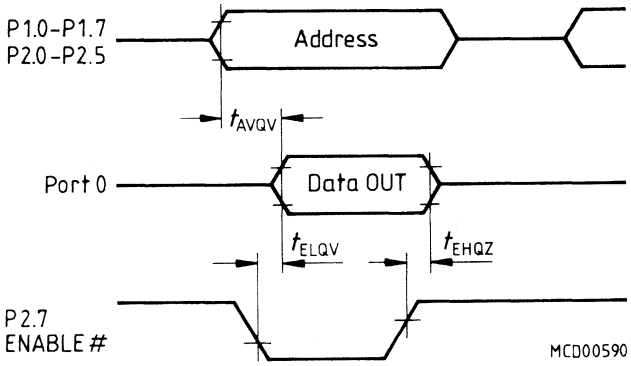


ROM Verification Characteristics

T_A = 25 °C ± 5 °C; V_{CC} = 5 V ± 10 %; V_{SS} = 0 V

Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	ENABLE to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after ENABLE	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	12	MHz

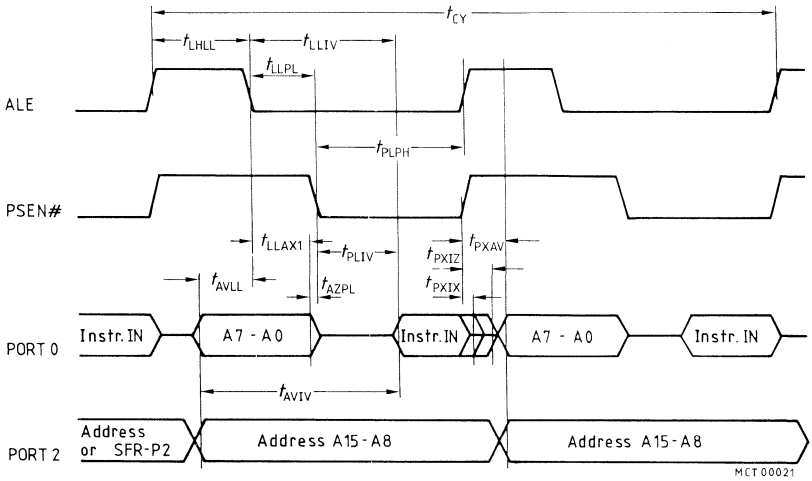
ROM Verification



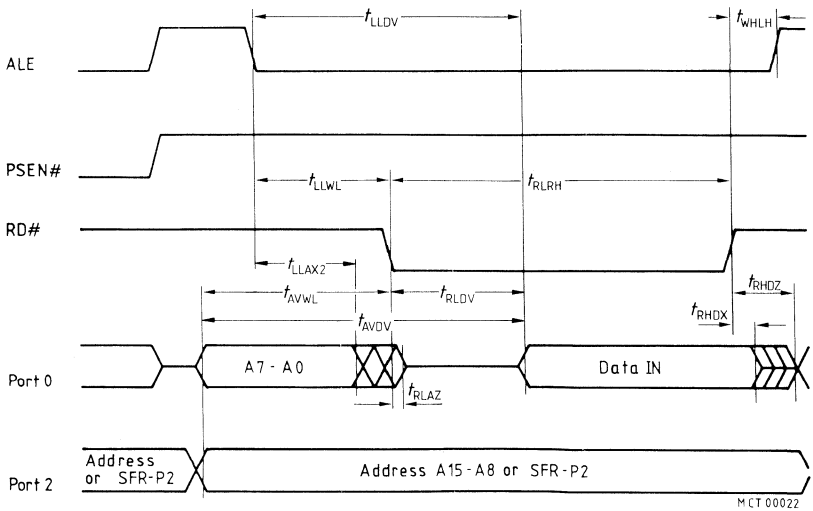
Address:	P1.0-P1.7	= A0-A7
	P2.0-P2.5	= A8-A13
Data:	Port 0	= D0-D7
Inputs:	P2.6, PSEN#	= V_{SS}
	ALE, EA#	= V_{IH}
	RESET#	= V_{IL}

Waveforms

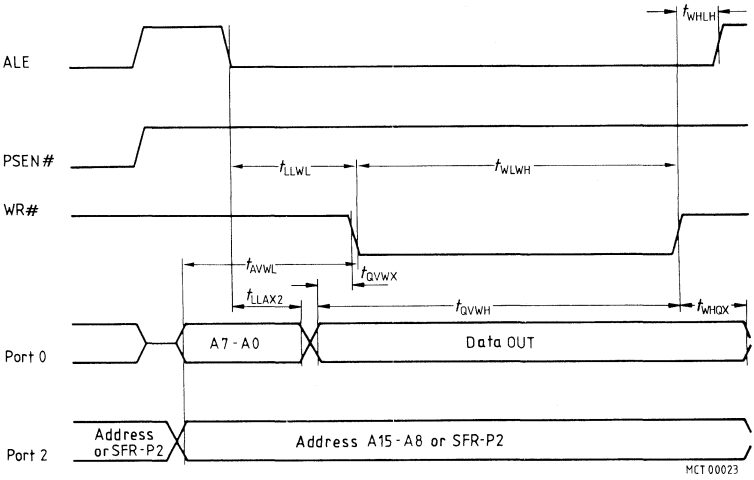
Program Memory Read Cycle



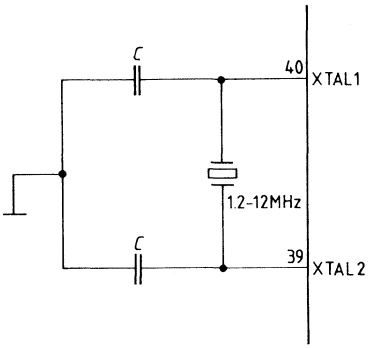
Data Memory Read Cycle



Data Memory Write Cycle

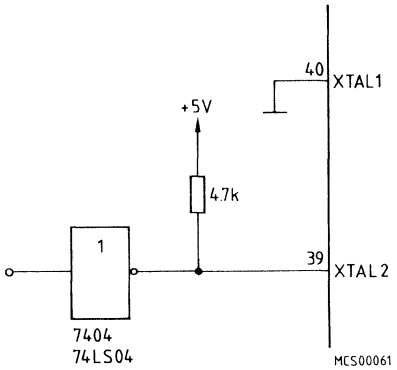


Recommended Oscillator Circuits



$C = 30pF \pm 10pF$

Crystal Oscillator Mode



Driving from External Source

16-Bit-Single Chip Microcontrollers

High-Performance 16-Bit CMOS Single-Chip Microcontrollers for Embedded Control Applications

SAB 80C166/83C166

Advance Information

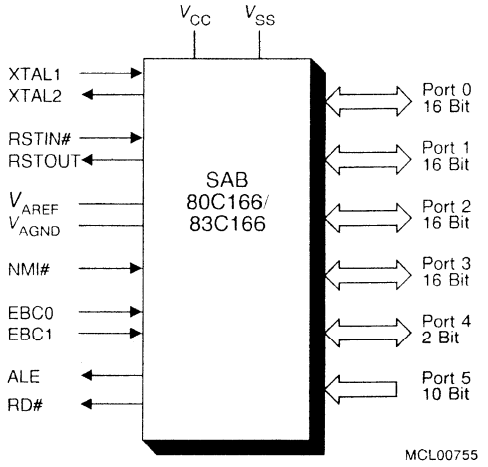
SAB 83C166-3S **16-bit Microcontroller with 8K Mask-Programmable ROM**
SAB 80C166-S **16-bit Microcontroller for External Program Memory**

- High Performance 16-bit CPU with 4-Stage Pipeline
- 100 ns Instruction Cycle Time at 20 MHz CPU clock
- 500 ns Multiplication (16×16 bits), 1 µs Division (32-/16 bit)
- Enhanced Boolean Bit Manipulation Facilities
- Register-Based Design with Multiple Variable Register Banks
- Single-Cycle Context Switching Support
- 256 Kbytes Linear Address Space for Code and Data
- 1 Kbyte On-Chip RAM
- 8 Kbytes On-Chip ROM (for the SAB 83C166, only)
- 512 bytes On-Chip Special Function Register Area
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- 16-Priority-Level Interrupt System
- 10-Channel 10-bit A/D Converter with 9.75 µs Conversion Time
- 16-Channel Capture/Compare Unit
- 2 Multi-Functional General Purpose Timer Units
- 2 Serial Channels (USARTs)
- Programmable Watchdog Timer
- 76 General Purpose I/O Lines
- Temperature Range: 0 to 70 °C (in preparation: – 40 to 85 °C, – 40 to 110 °C)
- 1.2 micron Siemens Low-Power CMOS Process
- Complete Set of Development Tools 'C'-Compiler, Macro Assembler, Linker, Locater, Librarian, Simulator, Emulator, Evaluation Board
- 100 Pin Plastic Quad Flat Pack (PQFP) Package

Introduction

The SAB 80C166 and the SAB 83C166 are the first representatives of the new Siemens SAB 80C166 family of full featured single-chip CMOS microcontrollers. They combine high CPU performance (up to 10 million instructions per second) with high peripheral functionality.

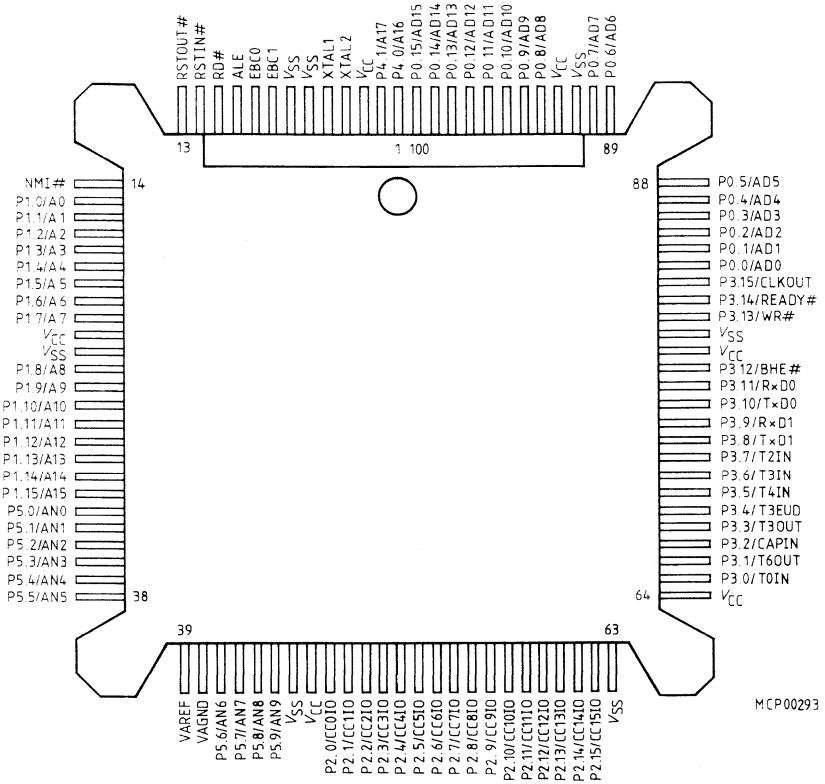
Figure 1
Logic Symbol



Ordering Information

Type	Ordering code	Package	Function
SAB 83C166-3S	Q67120-C552	P-QFP-100	16-bit microcontroller with 8 K mask-programmable ROM
SAB 80C166-S	Q67120-C493	P-QFP-100	16-bit microcontroller for external program memory

Figure 2
Pin Configuration (Top View)



Pin Definitions and Functions

Symbol	Pin Number	Input (I) Output (O)	Function
P4.0 - P4.1	1.2	I/O	Port 4 is a 2-bit bidirectional I/O port. It is bit-wise programmable for input or output via a direction bit. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, Port 4 is used for output of the two segment address lines supposed that segmentation is enabled:
	1 2	O O	P4.0 A16 Lower segment address line P4.1 A17 Higher segment address line
XTAL1	5	I	XTAL1: Input to the oscillator amplifier and input to the internal clock generator
XTAL2	4	O	XTAL2: Output of the oscillator amplifier circuits. To drive the device from an external source, XTAL1 should be driven while XTAL2 is left unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.
EBC0 EBC1	9 8	I I	External Bus Configuration selection inputs. These pins are sampled during reset and select either the single chip mode or one of the three external bus configurations, as follows: EBC1 EBC0 Mode Bus Configuration 0 0 Single Chip Mode 1 1 16/18-bit addresses, 8-bit data, multiplexed bus 1 0 16/18-bit addresses, 16-bit data, multiplexed bus 1 1 16/18-bit addresses, 16-bit data, non-multiplexed bus
RSTIN#	12	I	Reset Input with Schmitt-Trigger characteristics. A low level at this pin for a specified duration while the oscillator is running resets the SAB 80C166/83C166. An internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}
RSTOUT#	13	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. RSTOUT# remains low until the EINIT (end of initialization) instruction is executed.
NMI#	14	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the NMI# pin must be low in order to force the SAB 80C166/83C166 to go into power down mode. If NMI# is high when PWRDN is executed, the part will continue to run in normal mode.
ALE	10	O	Address latch enable output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
RD#	11	O	External memory read control signal. RD# is activated for every external instruction or data read access.

Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Input (I) Output (O)	Function
P1.0 - P1.15	15 - 22 25 - 32	I/O	Port 1 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via a direction bit. For a pin configured as input, the output driver is put into high-impedance state. Port 1 is also used as the 16-bit address bus (A) in the non-multiplexed bus mode.
	15 - 22 25 - 32	O O	16-bit address bus, non multiplexed: P1.0 - P1.15 A0 - A15
P5.0 - P5.9	33 - 38 41 - 44	I I	Port 5 is a 10-bit input port with Schmitt-Trigger characteristics. The pins of Port 5 are also used as the analog input channels for the A/D converter as listed below:
	33	I	P5.0 AN0 Analog input channel 0
	34	I	P5.1 AN1 Analog input channel 1
	35	I	P5.2 AN2 Analog input channel 2
	36	I	P5.3 AN3 Analog input channel 3
	37	I	P5.4 AN4 Analog input channel 4
	38	I	P5.5 AN5 Analog input channel 5
	41	I	P5.6 AN6 Analog input channel 6
	42	I	P5.7 AN7 Analog input channel 7
	43	I	P5.8 AN8 Analog input channel 8
	44	I	P5.9 AN9 Analog input channel 9
P2.0 - P2.15	47 - 62	I/O	Port 2 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via a direction bit. For a pin configured as input, the output driver is put into high-impedance state. The pins of Port 2 are also used as the capture inputs or compare outputs for the CAPCOM unit as listed in the following table:
	47	I/O	P2.0 CC0IO Register CC0 capture input/compare output
	48	I/O	P2.1 CC1IO Register CC1 capture input/compare output
	49	I/O	P2.2 CC2IO Register CC2 capture input/compare output
	50	I/O	P2.3 CC3IO Register CC3 capture input/compare output
	51	I/O	P2.4 CC4IO Register CC4 capture input/compare output
	52	I/O	P2.5 CC5IO Register CC5 capture input/compare output
	53	I/O	P2.6 CC6IO Register CC6 capture input/compare output
	54	I/O	P2.7 CC7IO Register CC7 capture input/compare output
	55	I/O	P2.8 CC8IO Register CC8 capture input/compare output
	56	I/O	P2.9 CC9IO Register CC9 capture input/compare output
	57	I/O	P2.10 CC10IO Register CC10 capture input/compare output
	58	I/O	P2.11 CC11IO Register CC11 capture input/compare output
	59	I/O	P2.12 CC12IO Register CC12 capture input/compare output
	60	I/O	P2.13 CC13IO Register CC13 capture input/compare output
	61	I/O	P2.14 CC14IO Register CC14 capture input/compare output
	62	I/O	P2.15 CC15IO Register CC15 capture input/compare output
P3.0 - P3.15	65-77 80-82	I/O I/O	Port 3 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via a direction bit. For a pin configured as input, the output driver is put into high-impedance state. The pins of Port 3 are also used for various functions such as timer inputs and outputs and bus control signals. The alternate functions of the Port 3 pins are listed in the following:

Pin Definitions and Functions (cont'd)

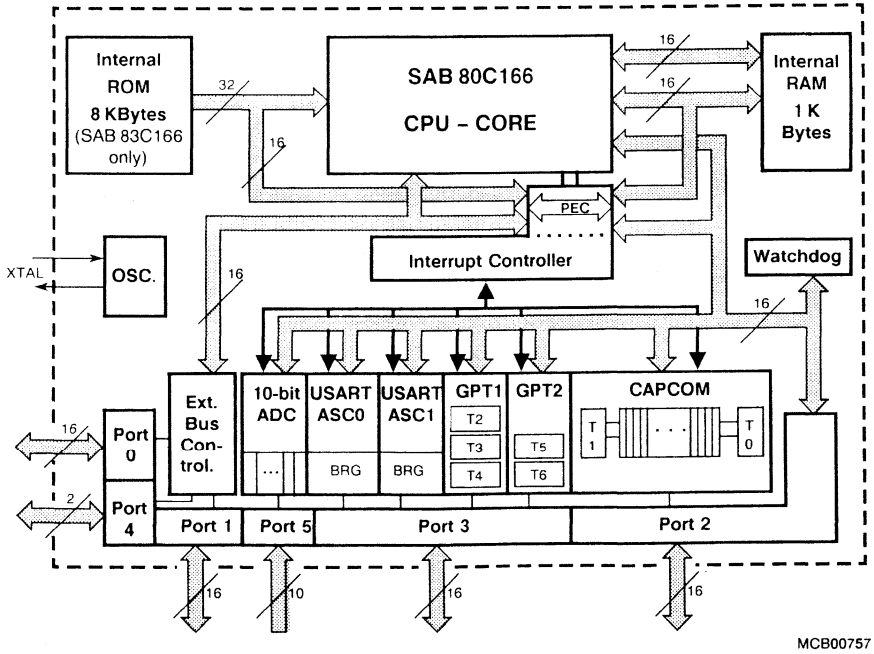
Symbol	Pin Number	Input (I) Output (O)	Function		
P3.0 - P3.15 (cont'd)	65	I	P3.0	T0IN	Timer 0 count input
	66	O	P3.1	T6OUT	Timer 6 toggle latch output
	67	I	P3.2	CAPIN	CAPREL register capture input
	68	O	P3.3	T3OUT	Timer 3 toggle latch output
	69	I	P3.4	T3EUD	Timer 3 external up/down control input
	70	I	P3.5	T4IN	Timer 4 count/gate/reload/capture input
	71	I	P3.6	T3IN	Timer 3 count/gate/input
	72	I	P3.7	T2IN	Timer 2 count/gate/reload/capture input
	73	O	P3.8	TxD1	Serial Channel 1 clock output in synchronous mode; data output in asynchronous mode
	74	I/O	P3.9	RxD1	Serial Channel 1 data input/output in synchronous mode; data input in asynchronous mode
	75	O	P3.10	TxD0	Serial Channel 0 clock output in synchronous mode; data output in asynchronous mode
	76	I/O	P3.11	RxD0	Serial Channel 0 data input/output in synchronous mode; data input in asynchronous mode
	77	O	P3.12	BHE#	External memory byte enable control signal
	80	O	P3.13	WR#	External memory write control signal
	81	I	P3.14	READY#	Ready input
	82	O	P3.15	CLKOUT	System clock output (oscillator frequency/2)
P0.0 - P0.15	83 - 90 93 - 100	I/O O	Port 0 is a 16-bit bidirectional I/O port. In case of the Single Chip Mode, Port 0 is bit-wise programmable for input or output via a direction bit. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, Port 0 serves as the address (A) and address/data (AD) bus in the multiplexed bus modes and as the data (D) bus in the non-multiplexed bus mode.		
			16-/18-bit addresses, 8-bit data, multiplexed bus:		
	83 - 90	I/O	P0.0 - P0.7	AD0 - AD7	
	93 - 100	O	P0.8 - P0.15	A8 - A15	
			16-/18-bit addresses, 16-bit data, multiplexed bus:		
	83 - 90 93 - 100	I/O	P0.0 - P0.15	AD0 - AD15	
			16-/18-bit addresses, 16-bit data, non-multiplexed bus:		
	83 - 90 93 - 100	I/O	P0.0 - P0.15	D0 - D15	
V_{CC}	3, 23, 46, 64 78, 92		Digital supply voltage: + 5 V during normal operation and idle mode ≥ 2.5 V during power down mode		
V_{SS}	6, 7, 24 45, 63, 79, 91		Digital ground		
V_{AREF}	39		Reference voltage for the A/D converter		
V_{AGND}	40		Reference ground for the A/D converter		

Functional Description

The architecture of the SAB 80C166 combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the SAB 80C166.

Note: In this description, any reference to the SAB 80C166 also applies to the SAB 83C166 unless otherwise noted. All time specifications refer to a CPU clock of 20 MHz which means an oscillator frequency (f_{OSC}) of 40 MH7.

Figure 3
Block Diagram



Memory Organization

The memory space of the SAB 80C166 is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which currently includes 256 Kbytes. Address space expansion to 16 Mbytes is provided for future versions. The entire memory space can be accessed bytewise or wordwise. Particular portions of the on-chip memory have additionally been made directly bit addressable.

The SAB 83C166 contains 8 Kbytes of a mask-programmable on-chip ROM for code or constant data.

A large dual port RAM of 1 Kbyte is contained on both the SAB 80C166 and the SAB 83C166. This internal RAM is provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, . . ., RL7, RH7) so called General Purpose Registers (GPRs).

512 bytes of the address space are reserved for the Special Function Register (SFR) area. SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. 98 SFRs are currently implemented. Unused SFR addresses are reserved for future members of the SAB 80C166 family.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 256 Kbytes of external RAM and/or ROM can be connected to the microcontroller.

External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed to either the Single Chip Mode when no external memory is required, or to one of three different external memory access modes, which are as follows:

– 16-/18-bit Addresses, 16-bit Data, Non-Multiplexed

– 16-/18-bit Addresses, 16-bit Data, Multiplexed

– 16-/18-bit Addresses, 8-bit Data, Multiplexed

In the non-multiplexed bus mode, Port 1 is used as an output for addresses and Port 0 is used as an input/output for data. In the multiplexed bus modes, just one of the two 16-bit ports, Port 0, is used as an input/output for both addresses and data.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time and Read write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories. Access to very slow memories is supported via a particular 'Ready' function.

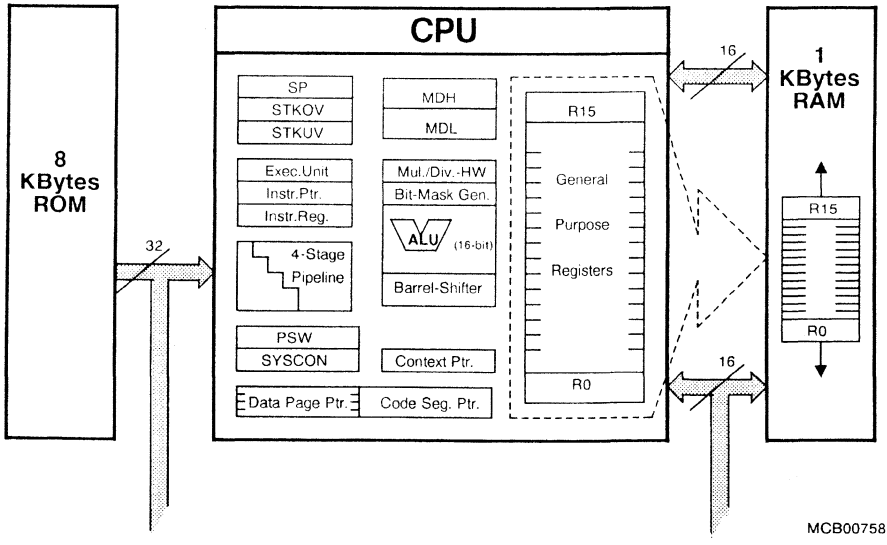
For applications which require less than 64 Kbytes of memory space, a non-segmented memory model can be selected. In this case, all memory locations can be addressed by 16 bits, and thus Port 4 is not needed as an output for the two most significant address bits (A17 and A16), as is the case when using the segmented memory model.

Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the SAB 80C166's instructions can be executed in just one machine cycle which requires 100 ns at 20 MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: A 32-/16 bit division in 1 µs, a 16 × 16 bit multiplication in 0.5 µs, and branches in 200 ns. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 200 ns to 100 ns.

Figure 4
CPU Block Diagram



The CPU disposes of an actual register context consisting of up to 16 wordwide GPRs which are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at the time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, register banks can also be organized overlappingly.

A system stack of up to 512 bytes is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly functional SAB 80C166 instruction set which includes the following instruction classes:

- Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

Interrupt System

With an interrupt response time within a range from just 250 ns to 600 ns (in case of internal program execution), the SAB 80C166 is capable of reacting very fast to the occurence of non-deterministic events.

The architecture of the SAB 80C166 supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data, or for transferring A/D converted results to a memory table. The SAB 80C166 has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized servise request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

The following table shows all of the possible SAB 80C166 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers:

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 0	CC0IR	CC0IE	CC0INT	40h	10h
CAPCOM Register 1	CC1IR	CC1IE	CC1INT	44h	11h
CAPCOM Register 2	CC2IR	CC2IE	CC2INT	48h	12h
CAPCOM Register 3	CC3IR	CC3IE	CC3INT	4Ch	13h
CAPCOM Register 4	CC4IR	CC4IE	CC4INT	50h	14h
CAPCOM Register 5	CC5IR	CC5IE	CC5INT	54h	15h
CAPCOM Register 6	CC6IR	CC6IE	CC6INT	58h	16h
CAPCOM Register 7	CC7IR	CC7IE	CC7INT	5Ch	17h
CAPCOM Register 8	CC8IR	CC8IE	CC8INT	60h	18h
CAPCOM Register 9	CC9IR	CC9IE	CC9INT	64h	19h
CAPCOM Register 10	CC10IR	CC10IE	CC10INT	68h	1Ah
CAPCOM Register 11	CC11IR	CC11IE	CC11INT	6Ch	1Bh
CAPCOM Register 12	CC12IR	CC12IE	CC12INT	70h	1Ch
CAPCOM Register 13	CC13IR	CC13IE	CC13INT	74h	1Dh
CAPCOM Register 14	CC14IR	CC14IE	CC14INT	78h	1Eh
CAPCOM Register 15	CC15IR	CC15IE	CC15INT	7Ch	1Fh
CAPCOM Timer 0	T0IR	T0IE	T0INT	80h	20h
CAPCOM Timer 1	T1IR	T1IE	T1INT	84h	21h
GPT 1 Timer 2	T2IR	T2IE	T2INT	88h	22h
GPT 1 Timer 3	T3IR	T3IE	T3INT	8Ch	23h
GPT 1 Timer 4	T4IR	T4IE	T4INT	90h	24h
GPT 2 Timer 5	T5IR	T5IE	T5INT	94h	25h
GPT 2 Timer 6	T6IR	T6IE	T6INT	98h	26h
GPT 2 CAPREL Register	CRIR	CRIE	CRINT	9Ch	27h
A/D Conversion Complete	ADCIR	ADCIE	ADCINT	A0h	28h
A/D Overrun Error	ADEIR	ADEIE	ADEINT	A4h	29h
Serial Channel 0 Tansmit	S0TIR	S0TIE	S0TINT	A8h	2Ah
Serial Channel 0 Receive	S0RIR	S0RIE	S0RINT	ACh	2Bh
Serial Channel 0 Error	S0EIR	S0EIE	S0EINT	B0h	2Ch
Serial Channel 1 Transmit	S1TIR	S1TIE	S1TINT	B4h	2Dh
Serial Channel 1 Receive	S1RIR	S1RIE	S1RINT	B8h	2Eh
Serial Channel 1 Error	S1EIR	S1EIE	S1EINT	BCh	2Fh

The SAB 80C166 also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called 'HardwareTraps'. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location).
The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except another higher prioritized trap service being in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

The following table shows all of the possible exceptions or error conditions that can arise during run-time:

Exception Condition	**Trap Flag**	**Trap Vector**	**Vector Location**	**Trap Number**	**Trap Priority**
Reset Functions:					
Hardware Reset		RESET	0h	0h	III
Software Reset		RESET	0h	0h	III
Watchdog Timer Overflow		RESET	0h	0h	III
Class A Hardware Traps:					
Non-Maskable Interrupt	NMI	NMITRAP	08h	2h	II
Stack Overflow	STKOF	STOTRAP	10h	4h	II
Stack Underflow	STKUF	STUTRAP	18h	6h	II
Class B Hardware Traps:					
Undefined Opcode	UNDOPC	BTRAP	28h	Ah	I
Protected Instruction Fault	PRTFLT	BTRAP	28h	Ah	I
Illegal Word Operand Access	ILLOPA	BTRAP	28h	Ah	I
Illegal Instruction Access	ILLINA	BTRAP	28h	Ah	I
Illegal External Bus Access	ILLBUS	BTRAP	28h	Ah	I
Reserved			[2Ch - 3Ch]	[Bh - Fh]	
Software Traps TRAP Instruction			Any [0h - 1FCh] in steps of 4H	Any [0h - 7Fh]	Current CPU Priority

Capture/Compare (CAPCOM) Unit

The CAPCOM unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of 400 ns. The CAPCOM unit is typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Two 16-bit timers (T0/T1) with reload registers provide two independent time bases for the capture/compare register array.

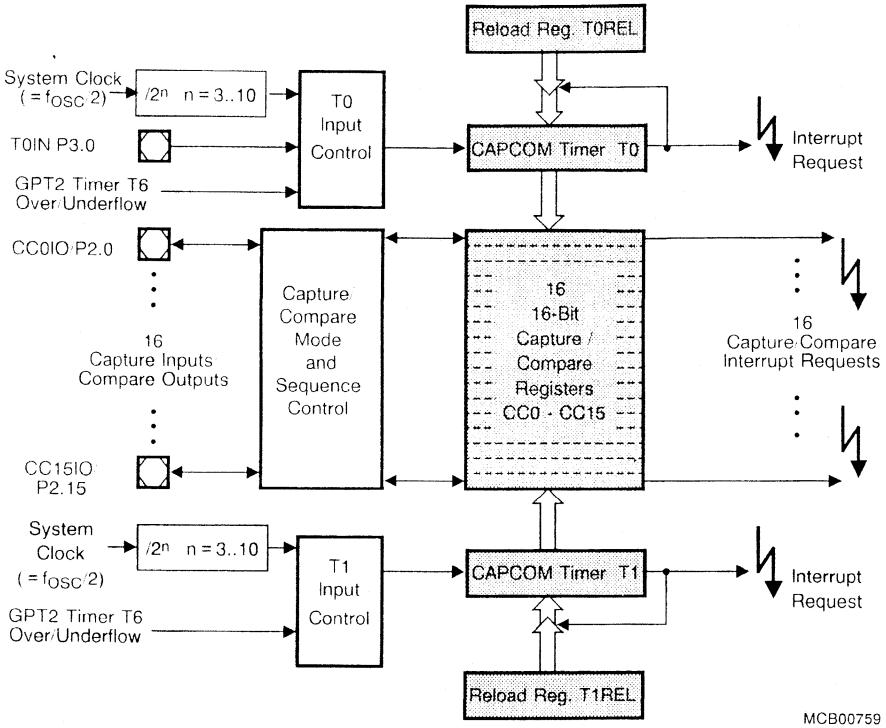
The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustment to the application specific requirements. In addition, an external count input for CAPCOM timer T0 allows event scheduling for the capture/compare registers relative to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1, and programmed for capture or compare function. Each register has one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('capture'd) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event. The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers. When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

Compare Modes	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated
Mode 3	Pin set to '1' on match; pin reset to '0' on compare time overflow; only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible.

Figure 5
CAPCOM Unit Block Diagram



General Purpose Timer (GPT) Unit

The GPT unit represents a very flexible multifunctional timer counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of the GPT1 module can be configured individually for one of three basic modes of operation, which are Timer, Gated Timer, and Counter Mode. In Timer Mode, the input clock for a timer is derived from the internal system clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (T2IN, T3IN, T4IN) which serves as gate or clock input. The maximum resolution of the timers in the GPT1 module is 400 ns (@f_{OSC} = 40 MHz).

The count direction (up/down) for each timer is programmable by software. For timer T3, the count direction may additionally be altered dynamically by an external signal on a port pin (T3EUD) to facilitate e. g. position tracking.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on a port pin (T3OUT) e. g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 are captured into T2 or T4 in response to a signal at their associated input pins (T2IN, T4IN). Timer T3 is reloaded with the contents of T2 or T4 either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

With its maximum resolution of 200 ns (@f_{OSC} = 40 MHz), the GPT2 module provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can independently count up or down, clocked with an input clock which is derived from a programmable prescaler. Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, or it may be output on a port pin (T6OUT). The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM timers T0 or T1, and to cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows absolute time differences to be measured or pulse multiplication to be performed without software overhead.

Figure 6
Block Diagram of GPT1

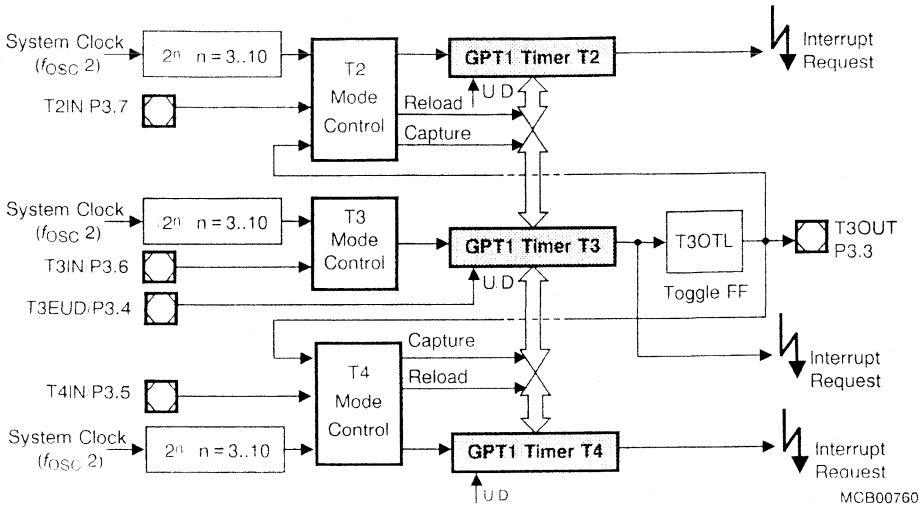
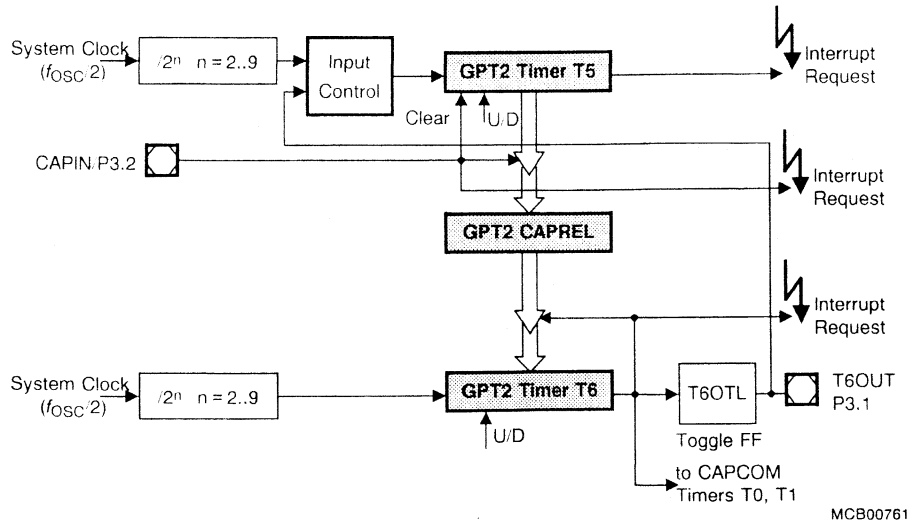


Figure 7
Block Diagram of GPT2



A/D Converter

For analog signal measurement, a 10-bit A/D converter with 10 multiplexed input channels and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation which returns the conversion result for an analog channel within 9.75 µs (@f_{OSC} = 40 MHz).

Overrun error detection capability is provided for the conversion result register (ADDAT): an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete.

For applications which require less than 10 analog input channels, the remaining channels can be used as digital input port pins.

The A/D converter of the SAB 80C166 supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is once sampled and converted into a digital result. In the Single Channel Continuous mode, the analog level is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels are sequentially sampled and converted. In the Auto Scan Continuous mode, the number of prespecified channels is repeatedly sampled and converted.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

Serial Channels

Serial communication with other microcontrollers, processors, terminals, or external peripheral components is provided by two serial interfaces with identical functionality, Serial Channel 0 (ASC0) and Serial Channel 1 (ASC1).

They are upward compatible with the serial ports of the Siemens SAB 8051x microcontroller family and support full-duplex asynchronous communication up to 625 Kbaud and half-duplex synchronous communication up to 2.5 Mbaud.

Two dedicated baud rate generators allow to set up all standard baud rates without oscillator tuning. For transmission, reception, and erroneous reception 3 separate interrupt vectors are provided for each serial channel.

In the synchronous mode, one data byte is transmitted or received synchronously to a shift clock which is generated by the SAB 80C166. In the asynchronous mode, an 8- or 9-bit data frame is transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data + wake up bit mode), and a loop back option is available for testing purposes.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated if the last character received has not been read out of the receive buffer register at the time reception of a new character is complete.

Watchdog Timer

The Watchdog Timer of the SAB 80C166 represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer of the SAB 80C166 is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. Thus, the chip'sstart-up procedure is always monitored. When the software has been designed to service the Watchdog Timer before it overflows, the Watchdog Timer times out if the program does not progress properly due to hardware or software related failures. When the Watchdog Timer overflows, it generates an internal hardware reset and pulls the RSTOUT# pin low in order to allow external hardware components to reset.

The Watchdog Timer of the SAB 80C166 is a 16-bit timer which can either be clocked with $f_{OSC}/4$ or $f_{OSC}/256$. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Thus, time intervals between 25 µs and 420 ms can be monitored (@f_{OSC} = 40 MHz). The default Watchdog Timer interval after reset is 6.55 ms.

Parallel Ports

The SAB 80C166 provides 76 I/O lines which are organized into four 16-bit I/O ports (Port 0 through 3), one 2-bit I/O port (Port 4), and one 10-bit input port (Port 5). All port lines are bit addressable, and all lines of Port 0 through 4 are individually bit-wise programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to the high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs.

Each port line has one programmable alternate input or output function associated with it. Ports 0 and 1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A16 and A17 in systems where segmentation is enabled to access more than 64 Kbytes of memory. Port 2 is associated with the capture inputs/compare outputs of the CAPCOM unit, and Port 3 includes alternate functions of timers, serial interfaces, optional bus control signals (WR#, BHE#, READY#), and the system clock output (CLKOUT). Port 5 is used for the analog input channels to the A/D converter. When anyone of these alternate functions is not used, the respective port line may be used as general purpose I/O line.

Instruction Set Summary

Mnemonic		Description	Bytes
Arithmetic operations			
ADD	Rw, Rw	Add direct word GPR to direct GPR	2
ADD	Rw, [Rw]	Add indirect word memory to direct GPR	2
ADD	Rw, [Rw +]	Add indirect word memory to direct GPR and post-increment source pointer by 2	2
ADD	Rw, #data3	Add immediate word data to direct GPR	2
ADD	reg, #data16	Add immediate word data to direct register	4
ADD	reg, mem	Add direct word memory to direct register	4
ADD	mem, reg	Add direct word register to direct memory	4
ADDB	Rb, Rb	Add direct byte GPR to direct GPR	2
ADDB	Rb, [Rw]	Add indirect byte memory to direct GPR	2
ADDB	Rb, [Rw +]	Add indirect byte memory to direct GPR and post-increment source pointer by 1	2
ADDB	Rb, #data3	Add immediate byte data to direct GPR	2
ADDB	reg, #data8	Add immediate byte data to direct register	4
ADDB	reg, mem	Add direct byte memory to direct register	4
ADDB	mem, reg	Add direct byte register to direct memory	4
ADDC	Rw, Rw	Add direct word GPR to direct GPR with Carry	2
ADDC	Rw, [Rw]	Add indirect word memory to direct GPR with Carry	2
ADDC	Rw, [Rw +]	Add indirect word memory to direct GPR with Carry and post-increment source pointer by 2	2
ADDC	Rw, #data3	Add immediate word data to direct GPR with Carry	2
ADDC	reg, #data16	Add immediate word data to direct register with Carry	4
ADDC	reg, mem	Add direct word memory to direct register with Carry	4
ADDC	mem, reg	Add direct word register to direct memory with Carry	4
ADDCB	Rb, Rb	Add direct byte GPR to direct GPR with Carry	2
ADDCB	Rb, [Rw]	Add indirect byte memory to direct GPR with Carry	2
ADDCB	Rb, [Rw +]	Add indirect byte memory to direct GPR with Carry and post-increment source pointer by 1	2

Instruction Set Summary

Mnemonic		Description	Bytes
Arithmetic operations (cont'd)			
ADDCB	Rb, #data3	Add immediate byte data to direct GPR with Carry	2
ADDCB	reg, #data8	Add immediate byte data to direct register with Carry	4
ADDCB	reg, mem	Add direct byte memory to direct register with Carry	4
ADDCB	mem, reg	Add direct byte register to direct memory with Carry	4
SUB	Rw, Rw	Subtract direct word GPR from direct GPR	2
SUB	Rw, [Rw]	Subtract indirect word memory from direct GPR	2
SUB	Rw, [Rw +]	Subtract indirect word memory from direct GPR and post-increment source pointer by 2	2
SUB	Rw, #data3	Subtract immediate word data from direct GPR	2
SUB	reg, #data16	Subtract immediate word data from direct register	4
SUB	reg, mem	Subtract direct word memory from direct register	4
SUB	mem, reg	Subtract direct word register from direct memory	4
SUBB	Rb, Rb	Subtract direct byte GPR from direct GPR	2
SUBB	Rb, [Rw]	Subtract indirect byte memory from direct GPR	2
SUBB	Rb, [Rw +]	Subtract indirect byte memory from direct GPR and post-increment source pointer by 1	2
SUBB	Rb, #data3	Subtract immediate byte data from direct GPR	2
SUBB	reg, #data8	Subtract immediate byte data from direct register	4
SUBB	reg, mem	Subtract direct byte memory from direct register	4
SUBB	mem, reg	Subtract direct byte register from direct memory	4
SUBC	Rw, Rw	Subtract direct word GPR from direct GPR with Carry	2
SUBC	Rw, [Rw]	Subtract indirect word memory from direct GPR with Carry	2
SUBC	Rw, [Rw +]	Subtract indirect word memory from direct GPR with Carry and post-increment source pointer by 2	2
SUBC	Rw, #data3	Subtract immediate word data from direct GPR with Carry	2
SUBC	reg, #data16	Subtract immediate word data from direct register with Carry	4
SUBC	reg, mem	Subtract direct word memory from direct register with Carry	4

Instruction Set Summary

Mnemonic		Description	Bytes
Arithmetic operations (cont'd)			
SUBC	mem, reg	Subract direct word register from direct memory with Carry	4
SUBCB	Rb, Rb	Subtract direct byte GPR from direct GPR with Carry	2
SUBCB	Rb, [Rw]	Subtract indirect byte memory from direct GPR with Carry	2
SUBCB	Rb, [Rw +]	Subtract indirect byte memory from direct GPR with Carry and post-increment source pointer by 1	2
SUBCB	Rb, #data3	Subtract immediate byte data from direct GPR with Carry	2
SUBCB	reg, #data8	Subtract immediate byte data from direct register with Carry	4
SUBCB	reg, mem	Subtract direct byte memory from direct register with Carry	4
SUBCB	mem, reg	Subtract direct byte register from direct memory with Carry	4
MUL	Rw, Rw	Signed multiply direct GPR by direct GPR (16-16-bit)	2
MULU	Rw, Rw	Unsigned multiply direct GPR by direct GPR (16-16-bit)	2
DIV	Rw	Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL	Rw	Signed long divide register MD by direct GPR (32-/16-bit)	2
DIVLU	Rw	Unsigned long divide register MD by direct GPR (32-/16-bit)	2
DIVU	Rw	Unsigned divide register MDL by direct GPR (16-/16-bit)	2
CPL	Rw	Complement direct word GPR	2
CPLB	Rb	Complement direct byte GPR	2
NEG	Rw	Negate direct word GPR	2
NEGB	Rb	Negate direct byte GPR	2

Instruction Set Summary

Mnemonic		Description	Bytes
Logical Instructions			
AND	Rw, Rw	Bitwise AND direct word GPR with direct GPR	2
AND	Rw, [Rw]	Bitwise AND indirect word memory with direct GPR	2
AND	Rw, [Rw +]	Bitwise AND indirect word memory with direct GPR and post-increment source pointer by 2	2
AND	Rw, #data3	Bitwise AND immediate word data with direct GPR	2
AND	reg, #data16	Bitwise AND immediate word data with direct register	4
AND	reg, mem	Bitwise AND direct word memory with direct register	4
AND	mem, reg	Bitwise AND direct word register with direct memory	4
ANDB	Rb, Rb	Bitwise AND direct byte GPR with direct GPR	2
ANDB	Rb, [Rw]	Bitwise AND indirect byte memory with direct GPR	2
ANDB	Rb, [Rw +]	Bitwise AND indirect byte memory with direct GPR and post-increment source pointer by 1	2
ANDB	Rb, #data3	Bitwise AND immediate byte data with direct GPR	2
ANDB	reg, #data8	Bitwise AND immediate byte data with direct register	4
ANDB	reg, mem	Bitwise AND direct byte memory with direct register	4
ANDB	mem, reg	Bitwise AND direct byte register with direct memory	4
OR	Rw, Rw	Bitwise OR direct word GPR with direct GPR	2
OR	Rw, [Rw]	Bitwise OR indirect word memory with direct GPR	2
OR	Rw, [Rw +]	Bitwise OR indirect word memory with direct GPR and post-increment source pointer by 2	2
OR	Rw, #data3	Bitwise OR immediate word data with direct GPR	2
OR	reg, #data16	Bitwise OR immediate word data with direct register	4
OR	reg, mem	Bitwise OR direct word memory with direct register	4
OR	mem, reg	Bitwise OR direct word register with direct memory	4

Instruction Set Summary

Mnemonic		Description	Bytes
Logical Instructions (cont'd)			
ORB	Rb, Rb	Bitwise OR direct byte GPR with direct GPR	2
ORB	Rb, [Rw]	Bitwise OR indirect byte memory with direct GPR	2
ORB	Rb, [Rw +]	Bitwise OR indirect byte memory with direct GPR and post-increment source pointer by 1	2
ORB	Rb, #data3	Bitwise OR immediate byte data with direct GPR	2
ORB	reg, #data8	Bitwise OR immediate byte data with direct register	4
ORB	reg, mem	Bitwise OR direct byte memory with direct register	4
ORB	mem, reg	Bitwise OR direct byte register with direct memory	4
XOR	Rw, Rw	Bitwise XOR direct word GPR with direct GPR	2
XOR	Rw, [Rw]	Bitwise XOR indirect word memory with direct GPR	2
XOR	Rw, [Rw +]	Bitwise XOR indirect word memory with direct GPR and post-increment source pointer by 2	2
XOR	Rw, #data3	Bitwise XOR immediate word data with direct GPR	2
XOR	reg, #data16	Bitwise XOR immediate word data with direct register	4
XOR	reg, mem	Bitwise XOR direct word memory with direct register	4
XOR	mem, reg	Bitwise XOR direct word register with direct memory	4
XORB	Rb, Rb	Bitwise XOR direct byte GPR with direct GPR	2
XORB	Rb, [Rw]	Bitwise XOR indirect byte memory with direct GPR	2
XORB	Rb, [Rw +]	Bitwise XOR indirect byte memory with direct GPR and post-increment source pointer by 1	2
XORB	Rb, #data3	Bitwise XOR immediate byte data with direct GPR	2
XORB	reg, #data8	Bitwise XOR immediate byte data with direct register	4
XORB	reg, mem	Bitwise XOR direct byte memory with direct register	4
XORB	mem, reg	Bitwise XOR direct byte register with direct memory	4

Instruction Set Summary

Mnemonic		Description	Bytes
Boolean bit manipulation operations			
BCLR	bitaddr	Clear direct bit	2
BSET	bitaddr	Set direct bit	2
BMOV	bitaddr, bitaddr	Move direct bit to direct bit	4
BMOVN	bitaddr, bitaddr	Move negated direct bit to direct bit	4
BAND	bitaddr, bitaddr	AND direct bit with direct bit	4
BOR	bitaddr, bitaddr	OR direct bit with direct bit	4
BXOR	bitaddr, bitaddr	XOR direct bit with direct bit	4
BCMP	bitaddr, bitaddr	Compare direct bit to direct bit	4
BFLDH	bitoff, #mask8, #data8	Bitwise modify masked high byte of bit-addressable direct word memory with immediate data	4
BFLDL	bitoff, #mask8, #data8	Bitwise modify masked low byte of bit-addressable direct word memory with immediate data	4
CMP	Rw, Rw	Compare direct word GPR to direct GPR	2
CMP	Rw, [Rw]	Compare indirect word memory to direct GPR	2
CMP	Rw, [Rw +]	Compare indirect word memory to direct GPR and post-increment source pointer by 2	2
CMP	Rw, #data3	Compare immediate word data to direct GPR	2
CMP	reg, #data16	Compare immediate word data to direct register	4
CMP	reg, mem	Compare direct word memory to direct register	4
CMPB	Rb, Rb	Compare direct byte GPR to direct GPR	2
CMPB	Rb, [Rw]	Compare indirect byte memory to direct GPR	2
CMPB	Rb, [Rw +]	Compare indirect byte memory to direct GPR and post-increment source pointer by 1	2
CMPB	Rb, #data3	Compare immediate byte data to direct GPR	2
CMPB	reg, #data8	Compare immediate byte data to direct register	4
CMPB	reg, mem	Compare direct byte memory to direct register	4

Instruction Set Summary

Mnemonic		Description	Bytes
Compare and Loop Control Instructions			
CMPD1	Rw, #data4	Compare immediate word data to direct GPR and decrement GPR by 1	2
CMPD1	Rw, #data16	Compare immediate word data to direct GPR and decrement GPR by 1	4
CMPD1	Rw, mem	Compare direct word memory to direct GPR and decrement GPR by 1	4
CMPD2	Rw, #data4	Compare immediate word data to direct GPR and decrement GPR by 2	2
CMPD2	Rw, #data16	Compare immediate word data to direct GPR and decrement GPR by 2	4
CMPD2	Rw, mem	Compare direct word memory to direct GPR and decrement GPR by 2	4
CMPI1	Rw, #data4	Compare immediate word data to direct GPR and increment GPR by 1	2
CMPI1	Rw, #data16	Compare immediate word data to direct GPR and increment GPR by 1	4
CMPI1	Rw. mem	Compare direct word memory to direct GPR and increment GPR by 1	4
CMPI2	Rw, #data4	Compare immediate word data to direct GPR and increment GPR by 2	2
CMPI2	Rw, #data16	Compare immediate word data to direct GPR and increment GPR by 2	4
CMPI2	Rw, mem	Compare direct word memory to direct GPR and increment GPR by 2	4
Prioritize Instruction			
PRIOR	Rw, Rw	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2

Instruction Set Summary

Mnemonic		Description	Bytes
Shift and Rotate Instructions			
SHL	Rw, Rw	Shift left direct word GPR; number of shift cycles specified by direct GPR	2
SHL	Rw, #data4	Shift left direct word GPR; number of shift cycles specified by immediate data	2
SHR	Rw, Rw	Shift right direct word GPR; number of shift cycles specified by direct GPR	2
SHR	Rw, #data4	Shift right direct word GPR; number of shift cycles specified by immediate data	2
ROL	Rw, Rw	Rotate left direct word GPR; number of shift cycles specified by direct GPR	2
ROL	Rw, #data4	Rotate left direct word GPR; number of shift cycles specified by immediate data	2
ROR	Rw, Rw	Rotate right direct word GPR; number of shift cycles specified by direct GPR	2
ROR	Rw, #data4	Rotate right direct word GPR; number of shift cycles specified by immediate data	2
ASHR	Rw, Rw	Arithmetic (sign bit) shift right direct word GPR; number of shift cycles specified by direct GPR	2
ASHR	Rw, #data4	Arithmetic (sign bit) shift right direct word GPR; number of shift cycles specified by immediate data	2
Data Movement			
MOV	Rw, Rw	Move direct word GPR to direct GPR	2
MOV	Rw, #data4	Move immediate word data to direct GPR	2
MOV	reg. #data16	Move immediate word data to direct register	4
MOV	Rw, [Rw]	Move indirect word memory to direct GPR	2
MOV	Rw, [Rw +]	Move indirect word memory to direct GPR and post-increment source pointer by 2	2
MOV	[Rw], Rw	Move direct word GPR to indirect memory	2
MOV	[-Rw], Rw	Pre-decrement destination pointer by 2 and move direct word GPR to indirect memory	2
MOV	[Rw], [Rw]	Move indirect word memory to indirect memory	2
MOV	[Rw +], [Rw]	Move indirect word memory to indirect memory and post-increment destination pointer by 2	2

Instruction Set Summary

Mnemonic		Description	Bytes
Data Movement (cont'd)			
MOV	[Rw], [Rw +]	Move indirect word memory to indirect memory and post-increment source pointer by 2	2
MOV	Rw, [Rw + #data16]	Move indirect word memory by base plus constant to direct GPR	4
MOV	[Rw + #data16], Rw	Move direct word GPR to indirect memory by base plus constant	4
MOV	[Rw], mem	Move direct word memory to indirect memory	4
MOV	mem, [Rw]	Move indirect word memory to direct memory	4
MOV	reg, mem	Move direct word memory to direct register	4
MOV	mem, reg	Move direct word register to direct memory	4
MOVB	Rb, Rb	Move direct byte GPR to direct GPR	2
MOVB	Rb, #data4	Move immediate byte data to direct GPR	2
MOVB	reg, #data16	Move immediate byte data to direct register	4
MOVB	Rb, [Rw]	Move indirect byte memory to direct GPR	2
MOVB	Rb, [Rw +]	Move indirect byte memory to direct GPR and post-increment source pointer by 1	2
MOVB	[Rw], Rb	Move direct byte GPR to indirect memory	2
MOVB	[-Rw], Rb	Pre-decrement destination pointer by 1 and move direct byte GPR to indirect memory	2
MOVB	[Rw], [Rw]	Move indirect byte memory to indirect memory	2
MOVB	[Rw +], [Rw]	Move indirect byte memory to indirect memory and post-increment destination pointer by 1	2
MOVB	[Rw], [Rw +]	Move indirect byte memory to indirect memory and post-increment source pointer by 1	2
MOVB	Rb, [Rw + #data16]	Move indirect byte memory by base plus constant to direct GPR	4
MOVB	[Rw + #data16], Rb	Move direct byte GPR to indirect memory by base plus constant	4
MOVB	[Rw], mem	Move direct byte memory to indirect memory	4
MOVB	mem, [Rw]	Move indirect byte memory to direct memory	4
MOVB	reg, mem	Move direct byte memory to direct register	4
MOVB	mem, reg	Move direct byte register to direct memory	4

Instruction Set Summary

Mnemonic		Description	Bytes
Data Movement (cont'd)			
MOVBS	Rw, Rb	Move direct byte GPR with sign extension to direct word GPR	2
MOVBS	reg, mem	Move direct byte memory with sign extension to direct word register	4
MOVBS	mem, reg	Move direct byte register with sign extension to direct word memory	4
MOVBZ	Rw, Rb	Move direct byte GPR with zero extension to direct word GPR	2
MOVBZ	reg, mem	Move direct byte memory with zero extension to direct word register	4
MOVBZ	mem, reg	Move direct byte register with zero extension to direct word memory	4
Jump and Call operations			
JMPA	cc, caddr	Jump absolute if condition is met	4
JMPI	cc, [Rw]	Jump indirect if condition is met	2
JMPR	cc, rel	Jump relative if condition is met	2
JMPS	seg, caddr	Jump absolute to a code segment	4
JB	bitaddr, rel	Jump relative if direct bit is set	4
JBC	bitaddr, rel	Jump relative and clear bit if direct bit is set	4
JNB	bitaddr, rel	Jump relative if direct bit is not set	4
JNBS	bitaddr, rel	Jump relative and set bit if direct bit is not set	4
CALLA	cc, caddr	Call absolute subroutine if condition is met	4
CALLI	cc, [Rw]	Call indirect subroutine if condition is met	2
CALLR	rel	Call relative subroutine	2
CALLS	seg, caddr	Call absolute subroutine in any code segment	4
PCALL	reg, caddr	Push direct word register onto system stack and call absolute subroutine	4
TRAP	#trap7	Call interrupt service routine via immediate trap number	2

Instruction Set Summary

Mnemonic		Description	Bytes
System Stack operations			
POP	reg	Pop direct word register from system stack	2
PUSH	reg	Push direct word register onto system stack	2
SCXT	reg, #data16	Push direct word register onto system stack und update register with immediate data	4
SCXT	reg, mem	Push direct word register onto system stack and update register with direct memory	4
Return operations			
RET		Return from intra-segment subroutine	2
RETS		Return from inter-segment subroutine	2
RETP	reg	Return from intra-segment subroutine and pop direct word register from system stack	2
RETI		Return from interrupt service subroutine	2
System Control			
SRST		Software Reset	4
IDLE		Enter Idle Mode	4
PWRDN		Enter Power Down Mode (supposes NMI#-Pin being low)	4
SRVWDT		Service Watchdog Timer	4
DISWDT		Disable Watchdog Timer	4
EINIT		Signify End-of-Initialization on RSTOUT-pin	4
Miscellaneous			
NOP		Null operation	2

Instruction Set Summary

Notes

Data addressing modes

Rw:	–	Word GPR (R0, R1, . . ., R15)
Rb:	–	Byte GPR (RL0, RH0, . . ., RL7, RH7)
reg:	–	SFR or GPR (in case of a byte operation on an SFR, only the low byte can be accessed via 'reg')
mem:	–	Direct word or byte memory location
[. . .]:	–	Indirect word or byte memory location (Any word GPR can be used as indirect address pointer, except for the arithmetic, logical and compare instructions, where only R0 to R3 are allowed)
bitaddr:	–	Direct bit in the bit-addressable memory area.
bitoff:	–	Direct word in the bit-addressable memory area.
#data:	–	Immediate constant (The number of significant bits which can be specified by the user is represented by the respective index 'i')
#mask8:	–	Immediate 8-bit mask used for bit-field modifications.

Multiply and divide operations

The MDL and MDH registers are implicit source and/or destination operands of the multiply and divide instructions.

Branch target addressing modes

caddr:	–	Direct 16-bit jump target address (Updates the Instruction Pointer)
seg:	–	Direct 2-bit segment address (Updates the Code Segment Pointer)
rel:	–	Signed 8-bit jump target word offset address relative to the Instruction Pointer of the following instruction
#trap7:	–	Immediate 7-bit trap or interrupt number.

Branch condition codes

cc:	Symbolically	specifiable condition codes
	cc_UC	– Unconditional
	cc_Z	– Zero
	cc_NZ	– Not Zero
	cc_V	– Overflow
	cc_NV	– No Overflow
	cc_N	– Negative
	cc_NN	– Not Negative
	cc_C	– Carry
	cc_NC	– No Carry
	cc_EQ	– Equal
	cc_NE	– Not Equal
	cc_ULT	– Unsigned Less Than
	cc_ULE	– Unsigned Less Than or Equal
	cc_UGE	– Unsigned Greater Than or Equal
	cc_UGT	– Unsigned Greater Than
	cc_SLE	– Signed Less Than or Equal
	cc_SGE	– Signed Greater Than or Equal
	cc_SGT	– Signed Greater Than
	cc_NET	– Not Equal and Not End-of-Table

Instruction Op Codes in Hexadecimal Order

Hex-code	Num-ber of bytes	Mnemonic	Operands
00	2	ADD	Rw, Rw
01	2	ADDB	Rb, Rb
02	4	ADD	reg, mem
03	4	ADDB	reg, mem
04	4	ADD	mem, reg
05	4	ADDB	mem, reg
06	4	ADD	reg, #data16
07	4	ADDB	reg, #data8
08	2	ADD	Rw, [Rw +] or Rw, [Rw] or Rw, #data3 [1]
09	2	ADDB	Rb, [Rw +] or Rb, [Rw] or Rb, #data3 [1]
0A	4	BFLDL	bitoff, #mask8, #data8
0B	2	MUL	Rw, Rw
0C	2	ROL	Rw, Rw
0D	2	JMPR	cc_UC, rel
0E	2	BCLR	bitoff.0
0F	2	BSET	bitoff.0
10	2	ADDC	Rw, Rw
11	2	ADDCB	Rb, Rb
12	4	ADDC	reg, mem
13	4	ADDCB	reg, mem
14	4	ADDC	mem, reg
15	4	ADDCB	mem, reg
16	4	ADDC	reg, #data16
17	4	ADDCB	reg, #data8
18	2	ADDC	Rw, [Rw +] or Rw, [Rw] or Rw, #data3 [1]
19	2	ADDCB	Rb, [Rw +] or Rb, [Rw] or Rb, #data3 [1]
1A	4	BFLDH	bitoff, #mask8 #data8
1B	2	MULU	Rw, Rw
1C	2	ROL	Rw, #data4
1D	2	JMPR	cc_NET, rel
1E	2	BCLR	bitoff.1
1F	2	BSET	bitoff.1
20	2	SUB	Rw, Rw
21	2	SUBB	Rb, Rb
22	4	SUB	reg, mem
23	4	SUBB	reg, mem
24	4	SUB	mem, reg
25	4	SUBB	mem, reg
26	4	SUB	reg, #data16
27	4	SUBB	reg, #data8
28	2	SUB	Rw, [Rw +] or Rw, [Rw] or Rw, #data3 [1]
29	2	SUBB	Rb, [Rw +] or Rb, [Rw] or Rb, #data3 [1]
2A	4	BCMP	bitaddr, bitaddr
2B	2	PRIOR	Rw, Rw
2C	2	ROR	Rw, Rw
2D	2	JMPR	cc_EQ, rel or cc_Z, rel
2E	2	BCLR	bitoff.2
2F	2	BSET	bitoff.2
30	2	SUBC	Rw, Rw
31	2	SUBCB	Rb, Rb
32	4	SUBC	reg, mem
33	4	SUBCB	reg, mem
34	4	SUBC	mem, reg
35	4	SUBCB	mem, reg

For notes see page 575

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex-code	Num-ber of bytes	Mnemonic	Operands
36	4	SUBC	reg, #data16
37	4	SUBCB	reg, #data8
38	2	SUBC	Rw, [Rw +] or Rw, [Rw] or Rw, #data3 [1]
39	2	SUBCB	Rb, [Rw +] or Rb, [Rw] or Rb, #data3 [1]
3A	4	BMOVN	bitaddr, bitaddr
3B	–	-----	-----
3C	2	ROR	Rw, #data4
3D	2	JMPR	cc_NE, rel or cc_NZ, rel
3E	2	BCLR	bitoff.3
3F	2	BSET	bitoff.3
40	2	CMP	Rw, Rw
41	2	CMPB	Rb, Rb
42	4	CMP	reg, mem
43	4	CMPB	reg, mem
44	–	-----	-----
45	–	-----	-----
46	4	CMP	reg, #data16
47	4	CMPB	reg, #data8
48	2	CMP	Rw, [Rw +] or Rw, [Rw] or Rw, #data3 [1])
49	2	CMPB	Rb, [Rw +] or Rb, [Rw] or Rb, #data3 [1]
4A	4	BMOV	bitadddr, bitaddr
4B	2	DIV	Rw
4C	2	SHL	Rw, Rw
4D	2	JMPR	cc_V, rel
4E	2	BCLR	bitoff.4
4F	2	BSET	bitoff.4

Hex-code	Num-ber of bytes	Mnemonic	Operands
50	2	XOR	Rw, Rw
51	2	XORB	Rb, Rb
52	4	XOR	reg, mem
53	4	XORB	reg, mem
54	4	XOR	mem, reg
55	4	XORB	mem, reg
56	4	XOR	reg, #data16
57	4	XORB	reg, #data8
58	2	XOR	Rw, [Rw +] or Rw, [Rw] or Rw, #data3 [1]
59	2	XORB	Rb, [Rw +] or Rb, [Rw] or Rb, #data3 [1]
5A	4	BOR	bitaddr, bitaddr
5B	2	DIVU	Rw
5C	2	SHL	Rw, #data4
5D	2	JMPR	cc_NV, rel
5E	2	BCLR	bitoff.5
5F	2	BSET	bitoff.5
60	2	AND	Rw, Rw
61	2	ANDB	Rb, Rb
62	4	AND	reg, mem
63	4	ANDB	reg, mem
64	4	AND	mem, reg
65	4	ANDB	mem, reg
66	4	AND	reg, #data16
67	4	ANDB	reg, #data8
68	2	AND	Rw, [Rw +] or Rw, [Rw] or Rw, #data3 [1]
69	2	ANDB	Rb, [Rw +] or Rb, [Rw] or Rb, #data3 [1]
6A	4	BAND	bitaddr, bitaddr

For notes see page 575

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex-code	Number of bytes	Mnemonic	Operands
6B	2	DIVL	Rw
6C	2	SHR	Rw, Rw
6D	2	JMPR	cc_N, rel
6E	2	BCLR	bitoff.6
6F	2	BSET	bitoff.6
70	2	OR	Rw, Rw
71	2	ORB	Rb, Rb
72	4	OR	reg, mem
73	4	ORB	reg, mem
74	4	OR	mem, reg
75	4	ORB	mem, reg
76	4	OR	reg, #data16
77	4	ORB	reg, #data8
78	2	OR	Rw, [Rw +] or Rw, [Rw] or Rw, #data3 [1]
79	2	ORB	Rb, [Rw +] or Rb, [Rw] or Rb, #data3 [1]
7A	4	BXOR	bitaddr, bitaddr
7B	2	DIVLU	Rw
7C	2	SHR	Rw, #data4
7D	2	JMPR	cc_NN, rel
7E	2	BCLR	bitoff.7
7F	2	BSET	bitoff.7
80	2	CMPI1	Rw, #data4
81	2	NEG	Rw
82	4	CMPI1	Rw, mem
83	-	-----	-----
84	4	MOV	[Rw], mem
85	-	-----	-----
86	4	CMPI1	Rw, #data16
87	4	IDLE	
88	2	MOV	[-Rw], Rw
89	2	MOVB	[-Rw], Rb
8A	4	JB	bitaddr, rel
8B	–	-----	-----
8C	–	-----	-----
8D	2	JMPR	cc_C, rel or cc_ULT, rel
8E	2	BCLR	bitoff.8
8F	2	BSET	bitoff.8
90	2	CMPI2	Rw, #data4
91	2	CPL	Rw
92	4	CMPI2	Rw, mem
93	–	-----	-----
94	4	MOV	mem, [Rw]
95	–	-----	-----
96	4	CMPI2	Rw, #data16
97	4	PWRDN	
98	2	MOV	Rw, [Rw +]
99	2	MOVB	Rb, [Rw +]
9A	4	JNB	bitaddr, rel
9B	2	TRAP	#trap7
9C	2	JMPI	cc, [Rw]
9D	2	JMPR	cc_NC, rel or cc_UGE, rel
9E	2	BCLR	bitoff.9
9F	2	BSET	bitoff.9
A0	2	CMPD1	Rw, #data4
A1	2	NEGB	Rb
A2	4	CMPD1	Rw, mem
A3	–	-----	-----
A4	4	MOVB	[Rw], mem
A5	4	DISWDT	

For notes see page 575

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex-code	Number of bytes	Mnemonic	Operands	Hex-code	Number of bytes	Mnemonic	Operands
A6	4	CMPD1	Rw, #data16	C6	4	SCXT	reg, #data16
A7	4	SRVWDT		C7	–	-----	-----
A8	2	MOV	Rw, [Rw]	C8	2	MOV	[Rw], [Rw]
A9	2	MOVB	Rb, [Rw]	C9	2	MOVB	[Rw], [Rw]
AA	4	JBC	bitaddr, rel	CA	4	CALLA	cc, caddr
AB	2	CALLI	cc, [Rw]	CB	2	RET	
AC	2	ASHR	Rw, Rw	CC	2	NOP	
AD	2	JMPR	cc_SGT, rel	CD	2	JMPR	cc_SLT, rel
AE	2	BCLR	bitoff.10	CE	2	BCLR	bitoff.12
AF	2	BSET	bitoff.10	CF	2	BSET	bitoff.12
B0	2	CMPD2	Rw, #data4	D0	2	MOVBS	Rw, Rb
B1	2	CPLB	Rb	D1	–	-----	-----
B2	4	CMPD2	Rw, mem	D2	4	MOVBS	reg, mem
B3	–	-----	-----	D3	–	-----	-----
B4	4	MOVB	mem, [Rw]	D4	4	MOV	Rw, [Rw +#data16]
B5	4	EINIT		D5	4	MOVBS	mem, reg
B6	4	CMPD2	Rw, #data16	D6	4	SCXT	reg, mem
B7	4	SRST		D7	–	-----	-----
B8	2	MOV	[Rw], Rw	D8	2	MOV	[Rw +], [Rw]
B9	2	MOVB	[Rw], Rb	D9	2	MOVB	[Rw +], [Rw]
BA	4	JNBS	bitaddr, rel	DA	4	CALLS	seg, caddr
BB	2	CALLR	rel	DB	2	RETS	
BC	2	ASHR	Rw, #data4	DC	–	-----	-----
BD	2	JMPR	cc_SLE, rel	DD	2	JMPR	cc_SGE, rel
BE	2	BCLR	bitoff.11	DE	2	BCLR	bitoff.13
BF	2	BSET	bitoff.11	DF	2	BSET	bitoff.13
C0	2	MOVBZ	Rw, Rb	E0	2	MOV	Rw, #data4
C1	–	-----	-----	E1	2	MOVB	Rb, #data4
C2	4	MOVBZ	reg, mem	E2	4	PCALL	reg, caddr
C3	–	-----	-----	E3	–	-----	-----
C4	4	MOV	[Rw +#data16], Rw	E4	4	MOVB	[Rw +#data16], Rb
C5	4	MOVBZ	mem, reg	E5	–	-----	-----

For notes see page 575

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex-code	Number of bytes	Mnemonic	Operands
E6	4	MOV	reg, #data16
E7	4	MOVB	reg, #data8
E8	2	MOV	[Rw], [Rw +]
E9	2	MOVB	[Rw], [Rw +]
EA	4	JMPA	cc, caddr
EB	2	RETP	reg
EC	2	PUSH	reg
ED	2	JMPR	cc_UGT, rel
EE	2	BCLR	bitoff.14
EF	2	BSET	bitoff.14
F0	2	MOV	Rw, Rw
F1	2	MOVB	Rb, Rb
F2	4	MOV	reg, mem
F3	4	MOVB	reg, mem
F4	4	MOVB	Rb, [Rw +#data16]
F5	–	-----	-----
F6	4	MOV	mem, reg
F7	4	MOVB	mem, reg
F8	–	-----	-----
F9	–	-----	-----
FA	4	JMPS	seg, caddr
FB	2	RETI	
FC	2	POP	reg
FD	2	JMPR	cc_ULE, rel
FE	2	BCLR	bitoff.15
FF	2	BSET	bitoff.15

Notes

1) These instructions are encoded by means of additional bits in the operand field of the instruction format. Thus, these instructions can be differentiated by means of the second byte, as follows:

x0h - x7h :	Rw, #data3	or	Rb, #data3
x8h - xBh :	Rw, [Rw]	or	Rb, [Rw]
xCH - xFh :	Rw, [Rw +]	or	Rb, [Rw +]

For these instructions, only the lowest four GPRs, R0 to R3, can be used as indirect address pointers.

Notes on the JMPR instructions

The condition code to be tested for the JMPR instructions is specified by the opcode.
Two mnemonic representation alternatives exist for some of the condition codes.

Notes on the BCLR and BSET instructions

The position of the bit to be set or to be cleared is specified by the opcode. The operand 'bitoff.n' (n = 0 to 15) refers to a particular bit within a bit-addressable word.

Notes on the undefined opcodes

A hardware trap occurs when one of the undefined opcodes signified by '-----' is decoded by the CPU.

Special Function Registers Overview

The following table lists all SFRs which are implemented in the SAB 80C166 in alphabetical order. Bit-addressable SFRs are marked with the letter "b" in column "Name". An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Name	Physical Address	8-bit Address	Description	Reset Value
ADCIC b	FF98h	CCh	A/D Converter End of Conversion Interrupt Control Register	0000h
ADCON b	FFA0h	D0h	A/D Converter Control Register	0000h
ADDAT	FEA0h	50h	A/D Converter Result Register	0000h
ADEIC b	FF9Ah	CDh	A/D Converter Overrun Error Interrupt Control Register	0000h
CAPREL	FE4Ah	25h	GPT2 Capture/Reload Register	0000h
CC0	FE80h	40h	CAPCOM Register 0	0000h
CC0IC b	FF78h	BCh	CAPCOM Register 0 Interrupt Control Register	0000h
CC1	FE82h	41h	CAPCOM Register 1	0000h
CC1IC b	FF7Ah	BDh	CAPCOM Register 1 Interrupt Control Register	0000h
CC2	FE84h	42h	CAPCOM Register 2	0000h
CC2IC b	FF7Ch	BEh	CAPCOM Register 2 Interrupt Control Register	0000h
CC3	FE86h	43h	CAPCOM Register 3	0000h
CC3IC b	FF7Eh	BFh	CAPCOM Register 3 Interrupt Control Register	0000h
CC4	FE88h	44h	CAPCOM Register 4	0000h
CC4IC b	FF80h	C0h	CAPCOM Register 4 Interrupt Control Register	0000h
CC5	FE8Ah	45h	CAPCOM Register 5	0000h
CC5IC b	FF82h	C1h	CAPCOM Register 5 Interrupt Control Register	0000h
CC6	FE8Ch	46h	CAPCOM Register 6	0000h
CC6IC b	FF84h	C2h	CAPCOM Register 6 Interrupt Control Register	0000h
CC7	FE8Eh	47h	CAPCOM Register 7	0000h
CC7IC b	FF86h	C3h	CAPCOM Register 7 Interrupt Control Register	0000h
CC8	FE90h	48h	CAPCOM Register 8	0000h
CC8IC b	FF88h	C4h	CAPCOM Register 8 Interrupt Control Register	0000h
CC9	FE92h	49h	CAPCOM Register 9	0000h
CC9IC b	FF8Ah	C5h	CAPCOM Register 9 Interrupt Control Register	0000h
CC10	FE94h	4Ah	CAPCOM Register 10	0000h
CC10IC b	FF8Ch	C6h	CAPCOM Register 10 Interrupt Control Register	0000h

Special Function Registers Overview (cont'd)

Name	Physical Address	8-bit Address	Description	Reset Value
CC11	FE96h	4Bh	CAPCOM Register 11	0000h
CC11IC b	FF8Eh	C7h	CAPCOM Register 11 Interrupt Control Register	0000h
CC12	FE98h	4Ch	CAPCOM Register 12	0000h
CC12IC b	FF90h	C8h	CAPCOM Register 12 Interrupt Control Register	0000h
CC13	FE9Ah	4Dh	CAPCOM Register 13	0000h
CC13IC b	FF92h	C9h	CAPCOM Register 13 Interrupt Control Register	0000h
CC14	FE9Ch	4Eh	CAPCOM Register 14	0000h
CC14IC b	FF94h	CAh	CAPCOM Register 14 Interrupt Control Register	0000h
CC15	FE9Eh	4Fh	CAPCOM Register 15	0000h
CC15IC b	FF96h	CBh	CAPCOM Register 15 Interrupt Control Register	0000h
CCM0 b	FF52h	A9h	CAPCOM Mode Control Register 0	0000h
CCM1 b	FF54h	AAh	CAPCOM Mode Control Register 1	0000h
CCM2 b	FF56h	ABh	CAPCOM Mode Control Register 2	0000h
CCM3 b	FF58h	ACh	CAPCOM Mode Control Register 3	0000h
CP	FE10h	08h	CPU Context Pointer Register	FC00h
CRIC b	FF6Ah	B5h	GPT2 CAPREL Interrupt Control Register	0000h
CSP	FE08h	04h	CPU Code Segment Pointer Register (2 bits, read only)	0000h
DP0 b	FF02h	81h	Port 0 Direction Control Register	0000h
DP1 b	FF06h	83h	Port 1 Direction Control Register	0000h
DP2 b	FFC2h	E1h	Port 2 Direction Control Register	0000h
DP3 b	FFC6h	E3h	Port 3 Direction Control Register	0000h
DP4 b	FF0Ah	85h	Port 4 Direction Control Register (2 bits)	0000h
DPP0	FE00h	00h	CPU Data Page Pointer 0 Register (4 bits)	0000h
DPP1	FE02h	01h	CPU Data Page Pointer 1 Register (4 bits)	0001h
DPP2	FE04h	02h	CPU Data Page Pointer 2 Register (4 bits)	0002h
DPP3	FE06h	03h	CPU Data Page Pointer 3 Register (4 bits)	0003h
MDC b	FF0Eh	87h	CPU Multiply Divide Control Register	0000h
MDH	FE0Ch	06h	CPU Multiply Divide Register – High Word	0000h
MDL	FE0Eh	07h	CPU Multiply Divide Register – Low Word	0000h
ONES	FF1Eh	8Fh	Constand Value 1's Register (read only)	FFFFh

Special Function Registers Overview (cont'd)

Name		Physical Address	8-bit Address	Description	Reset Value
P0	**b**	FF00h	80h	Port 0 Register	0000h
P1	**b**	FF04h	82h	Port 1 Register	0000h
P2	**b**	FFC0h	E0h	Port 2 Register	0000h
P3	**b**	FFC4h	E2h	Port 3 Register	0000h
P4	**b**	FF08h	84h	Port 4 Register (2 bits)	0000h
P5	**b**	FFA2h	D1h	Port 5 Register (10 bits, read only)	XXXXh
PECC0		FEC0h	60h	PEC Channel 0 Control Register	0000h
PECC1		FEC2h	61h	PEC Channel 1 Control Register	0000h
PECC2		FEC4h	62h	PEC Channel 2 Control Register	0000h
PECC3		FEC6h	63h	PEC Channel 3 Control Register	0000h
PECC4		FEC8h	64h	PEC Channel 4 Control Register	0000h
PECC5		FECAh	65h	PEC Channel 5 Control Register	0000h
PECC6		FECCh	66h	PEC Channel 6 Control Register	0000h
PECC7		FECEh	67h	PEC Channel 7 Control Register	0000h
PSW	**b**	FF10h	88h	CPU Program Status Word	0000h
S0BG		FEB4h	5Ah	Serial Channel 0 Baud Rate Generator Reload Register	0000h
S0CON	**b**	FFB0h	D8h	Serial Channel 0 Control Register	0000h
S0EIC	**b**	FF70h	D8h	Serial Channel 0 Error Interrupt Control Register	0000h
S0RBUF		FEB2h	59	Serial Channel 0 Receive Buffer Register (read only)	XXXXh
S0RIC	**b**	FF6Eh	B7h	Serial Channel 0 Receive Interrupt Control Register	0000h
S0TBUF		FEB0h	58h	Serial Channel 0 Transmit Buffer Register (write only)	0000h
S0TIC	**b**	FF6Ch	B6h	Serial Channel 0 Transmit Interrupt Control Register	0000h
S1BG		FEBCh	5Eh	Serial Channel 1 Baud Rate Generator Reload Register	0000h
S1CON	**b**	FFB8h	DCh	Serial Channel 1 Control Register	0000h
S1EIC	**b**	FF76h	BBh	Serial Channel 1 Error Interrupt Control Register	0000h
S1RBUF		FEBAh	5Dh	Serial Channel 1 Receive Buffer Register (read only)	XXXXh
S1RIC	**b**	FF74h	BAh	Serial Channel 1 Receive Interrupt Control Register	0000h
S1TBUF		FEB8h	5Ch	Serial Channel 1 Transmit Buffer Register (write only)	0000h
S1TIC	**b**	FF72h	B9h	Serial Channel 1 Transmit Interrupt Control Register	0000h
SP		FE12h	09h	CPU System Stack Pointer Register	FC00h

Special Function Registers Overview (cont'd)

Name	Physical Address	8-bit Address	Description	Reset Value
STKOV	FE14h	0Ah	CPU Stack Overflow Pointer Register	FA00h
STKUN	FE16h	0Bh	CPU Stack Underflow Pointer Register	FC00h
SYSCON b	FF0Ch	86h	CPU System Configuration Register	0XX0h*)
T0	FE50h	28h	CAPCOM Timer 0 Register	0000h
T01CON b	FF50h	A8h	CAPCOM Timer 0 and Timer 1 Control Register	0000h
T0IC b	FF9Ch	CEh	CAPCOM Timer 0 Interrupt Control Register	0000h
T0REL	FE54h	2Ah	CAPCOM Timer 0 Reload Register	0000h
T1	FE52h	29h	CAPCOM Timer 1 Register	0000h
T1IC b	FF9Eh	CFh	CAPCOM Timer 1 Interrupt Control Register	0000h
T1REL	FE56h	2Bh	CAPCOM Timer 1 Reload Register	0000h
T2	FE40h	20h	GPT1 Timer 2 Register	0000h
T2CON b	FF40h	A0h	GPT1 Timer 2 Control Register	0000h
T2IC b	FF60h	B0h	GPT1 Timer 2 Interrupt Control Register	0000h
T3	FE42h	21h	GPT1 Timer 3 Register	0000h
T3CON b	FF42h	A1h	GPT1 Timer 3 Control Register	0000h
T3IC b	FF62h	B1h	GPT1 Timer 3 Interrupt Control Register	0000h
T4	FE44h	22h	GPT1 Timer 4 Register	0000h
T4CON b	FF44h	A2h	GPT1 Timer 4 Control Register	0000h
T4IC b	FF64h	B2h	GPT1 Timer 4 Interrupt Control Register	0000h
T5	FE46h	23h	GPT2 Timer 5 Register	0000h
T5CON b	FF46h	A3h	GPT2 Timer 5 Control Register	0000h
T5IC b	FF66h	B3h	GPT2 Timer 5 Interrupt Control Register	0000h
T6	FE48h	24h	GPT2 Timer 6 Register	0000h
T6CON b	FF48h	A4h	GPT2 Timer 6 Control Register	0000h
T6IC b	FF68h	B4h	GPT2 Timer 6 Interrupt Control Register	0000h
TFR b	FFACh	D6h	Trap Flag Register	0000h
WDT	FEAEh	57h	Watchdog Timer Register (read only)	0000h
WDTCON	FFAEh	D7h	Watchdog Timer Control Register	0000h
ZEROS b	FF1Ch	8Eh	Constant Value 0's Register (read only)	0000h

*) system configuration selected during reset

Absolute Maximum Ratings

Ambient temperature under bias (T_A) ..... 0 to + 70 °C
Storage temperature (T_{ST}) ..... – 65 to + 150 °C
Supply Voltage (V_{CC}) ..... + 6.5 V
Input voltage (V_{IN} min. = – 3.0 V for pulse width less than 15 ns) ..... – 0.5 to V_{CC} + 0.5 V
Power dissipation ..... tbd

Notes *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

The SAB 80C166 will also be offered in the temperature ranges – 40 to + 110 °C and – 40 to + 85 °C.

All of the following time specifications refer to a CPU clock of 20 MHz which is identical to an oscillator frequency (f_{OSC}) of 40 MHz.

DC Characteristics

T_A = 0 to + 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	Limit Values		Unit	Test condition
		min.	max.		
V_{IL}	Input Low Voltage	– 0.5	0.2 V_{CC} – 0.1	V	–
V_{IH}	Input High Voltage (all except RSTIN# and XTAL1)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
V_{IH1}	Input High Voltage RSTIN#	0.6 V_{CC}	V_{CC} + 0.5	V	–
V_{IH2}	Input High Voltage XTAL1	0.7 V_{CC}	V_{CC} + 0.5	V	–
V_{OL}	Output Low Voltage (Ports 0, 1, 4, ALE, RD#, WR#, BHE#, CLKOUT, RSTOUT#)	–	0.4	V	I_{OL} = 2.4 mA
V_{OL1}	Output Low Voltage (all other outputs	–	0.4	V	I_{OL1} = 1.6 mA
V_{OH}	Output High Voltage Ports 0, 1, 4, ALE, RD#, WR#, BHE#, CLKOUT, RSTOUT#)	0.9 V_{CC} 2.4	–	V	I_{OH} = – 100 µA I_{OH} = – 2.4 mA
V_{OH1}	Output High Voltage (in all outputs)	0.9 V_{CC} 2.4	–	V V	I_{OH} = – 50 µA I_{OH} = – 1.6 mA
I_{OZ}	Input Leakage Current (Ports 0, 1, 2, 3, 4, NMI#, EBC0, EBC1)	–	±1	µA	0 V<V_{in}<V_{CC}

DC Characteristics (cont'd)

Symbol	Parameter	Limit Values		Unit	Test condition
		min.	max.		
R_{RST}	Reset Pullup Resistor	50	150	kΩ	–
I_{IL}	XTAL1 Input Current	–	tbd	µA	0 V<V_{in}<V_{CC}
C_{IO}	Pin Capacitance (digital inputs/outputs)	–	10	pF	f = 1 MHz T_A = 25 °C
I_{CC}	Power Supply Current	–	180	mA	1/TCL = 40 MHz
I_{ID}	Idle Mode Supply Current	–	20	mA	1/TCL = 40 MHz
I_{PD}	Power Down Mode Supply Current	–	100	µA	V_{CC} = 2.5 V 1)

A/D Converter Characteristics

T_A = 0 to +70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V; V_{AREF} = V_{CC} ± 0.2 V; V_{AGND} = V_{SS} ± 0.2 V

Symbol	Parameter	Limit Values		Unit	Test condition
		min.	max.		
V_{AIN}	Analog Input Voltage	V_{SS} – 0.2	V_{CC} + 0.2	V	–
C_I	Analog Input Capacitance	–	70	pF	–
t_S	Sample Time	–	63 TCL		2)
t_C	Conversion Time	–	390 TCL		3)
TUE	Total Unadjusted Error	–	± 2	LSB	–
I_{REF}	V_{AREF} Supply Current	–	5	mA	4)
I_{AIN}	Analog Input Current	–	± 500	nA	5)

Notes

1) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{CC} – 0.1 V to V_{CC}, V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.

2) This parameter specifies the time during which the input capacitance C_I can be charged/decharged by the external source. It must be guaranteed, that the input capacitance C_I is fully loaded within these 63 TCLs. 63 TCL is 1.575 µs at 20 MHz CPU clock. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time TS. 390 TCL is 9.75 µs at 20 MHz CPU clock.

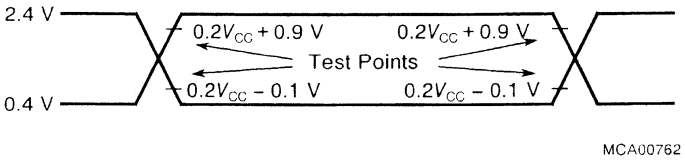
4) I_{REF} in Power Down Mode: TBD

5) This parameter specifies the static input current for an analog input channel, e. g. when the channel is not selected for conversion.

AC Characteristics

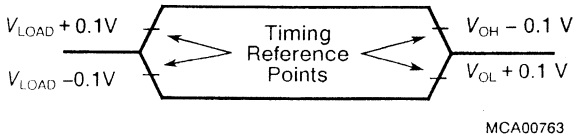
Testing Waveforms

Figure 8
Input Output Waveforms



AC Inputs during testing are driven at 2.4 V for a logic '1' and 0.4 V for a logic '0'. Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'.

Figure 9
Float Waveforms

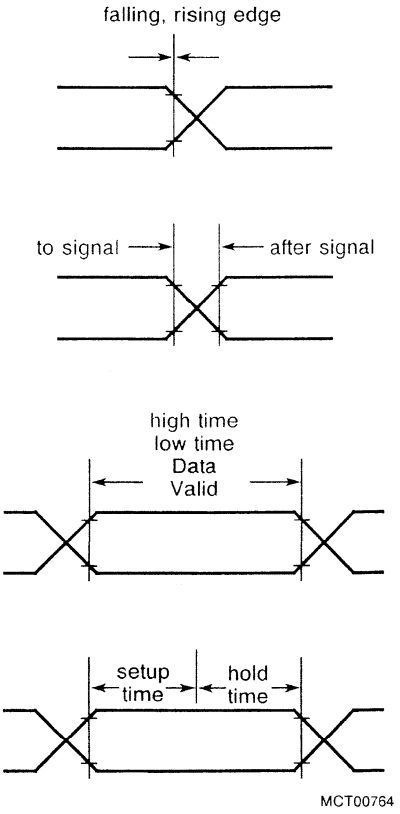


For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20 mA).

AC Characteristics (cont'd)

In the AC Characteristics waveforms, the mid-point of a signal transition is mostly used as the timing reference point. If not specifically specified in the drawings, the exact timing reference points are given by the parameter description according to the following figures (test voltage levels and float state references shown on previous page):

Figure 10
Timing Reference Points

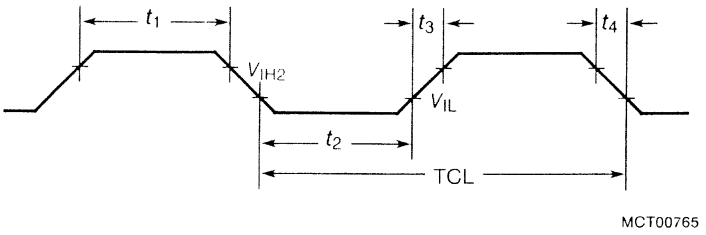


AC Characteristics (cont'd)

External Clock Drive XTAL1
T_A = 0 to + 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	CPU Clock 20 MHz		Variable Timing 1/TCL = 2 to 40 MHz		Unit
		min.	max.	min.	max.	
TCL	Oscillator Period	25	25	25	500	ns
t_1	High Time	6	–	6	–	ns
t_2	Low Time	6	–	6	–	ns
t_3	Rise Time	–	5	–	5	ns
t_4	Fall Time	–	5	–	5	ns

Figure 10
External Clock Drive XTAL1



AC Characteristics (cont'd)

Multiplexed Bus with Read/Write Delay
T_A = 0 to + 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V;
C_L (for Ports 0, 1 and 4, ALE, RD#, WR#, BHE#, CLKOUT) = 100 pF
ALE cycle time = 6 TCL (150 ns at 20 MHz CPU clock)

Symbol	Parameter	CPU Clock 20 MHz		Variable Timing 1/TCL = 2 to 40 MHz		Unit
		min.	max.	min.	max.	
t_5	ALE High Time	15	–	TCL – 10	–	ns
t_6	Address Setup to ALE	10	–	TCL – 15	–	ns
t_7	Address Hold after ALE	15	–	TCL – 10	–	ns
t_8	ALE Falling Edge to RD#, WR#	15	–	TCL – 10	–	ns
t_{10}	Address Float after RD#, WR#	–	5	–	5	ns
t_{12}	RD#, WR# Low Time	40	–	2TCL – 10	–	ns
t_{14}	RD# to Valid Data In	–	35	–	2TCL – 15	ns
t_{16}	ALE Low to Valid Data In	–	60	–	3TCL – 15	ns
t_{17}	Address to Valid Data In	–	75	–	4TCL – 25	ns
t_{18}	Data Hold after RD# Rising Edge	0	–	0	–	ns
t_{19}	Data Float after RD#	–	35	–	2TCL – 15	ns
t_{22}	Data Valid to WR#	35	–	2TCL – 15	–	ns
t_{23}	Data Hold after WR#	35	–	2TCL – 15	–	ns
t_{25}	ALE rising edge after RD#, WR#	35	–	2TCL – 15	–	ns
t_{27}	Address Hold after RD#, WR#	35	–	2TCL – 15	–	ns

Figure 11
External Memory Read Cycle

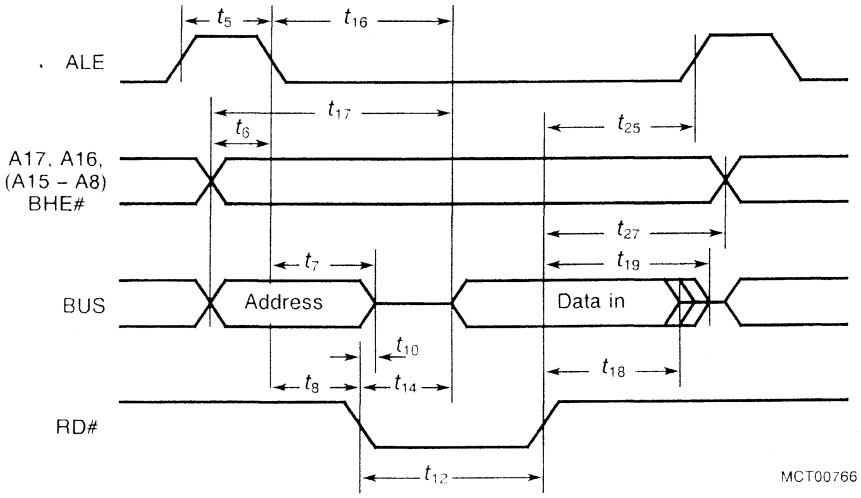
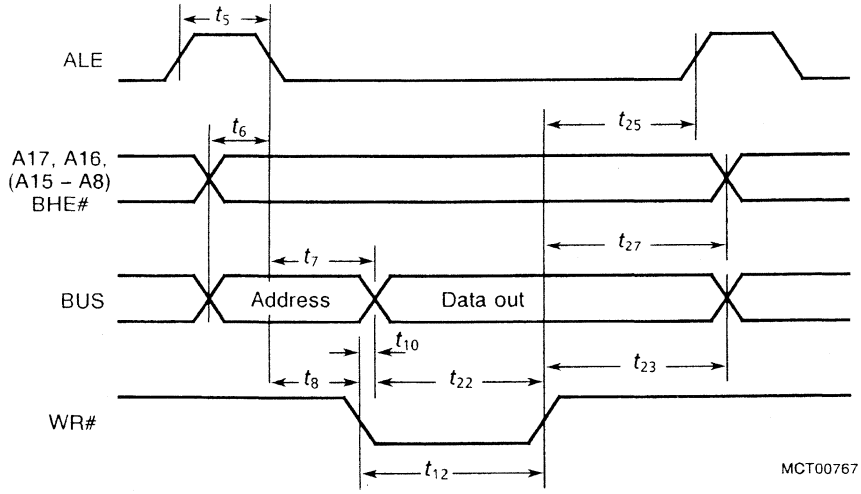


Figure 12
External Memory Write Cycle



AC Characteristics (cont'd)

Multiplexed Bus without Read/Write Delay
T_A = 0 to + 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V;
C_L (for Ports 0, 1 and 4, ALE, RD#, WR#, BHE#, CLKOUT) = 100 pF
ALE cycle time = 6 TCL (150 ns at 20 MHz CPU clock)

Symbol	Parameter	CPU Clock 20 MHz		Variable Timing 1/TCL = 2 to 40 MHz		Unit
		min.	max.	min.	max.	
t_5	ALE High Time	15	–	TCL – 10	–	ns
t_6	Address Setup to ALE	10	–	TCL – 15	–	ns
t_7	Address Hold after ALE	15	–	TCL – 10	–	ns
t_9	ALE Falling Edge to RD#, WR#	– 10	–	– 10	–	ns
t_{11}	Address Float after RD#, WR#	–	30	–	TCL + 5	ns
t_{13}	RD#, WR# Low Time	65	–	3TCL – 10	–	ns
t_{15}	RD# to Valid Data In	–	60	–	3TCL – 15	ns
t_{16}	ALE Low to Valid Data In	–	60	–	3TCL – 15	ns
t_{17}	Address to Valid Data In	–	75	–	4TCL – 25	ns
t_{18}	Data Hold after RD# Rising Edge	0	–	0	–	ns
t_{19}	Data Float after RD#	–	35	–	2TCL – 15	ns
t_{22}	Data Valid to WR#	35	–	2TCL – 15	–	ns
t_{23}	Data Hold after WR#	35	–	2TCL – 15	–	ns
t_{25}	ALE rising edge after RD#, WR#	35	–	2TCL – 15	–	ns
t_{27}	Address Hold after RD#, WR#	35	–	2TCL – 15	–	ns

Figure 13
External Memory Read Cycle

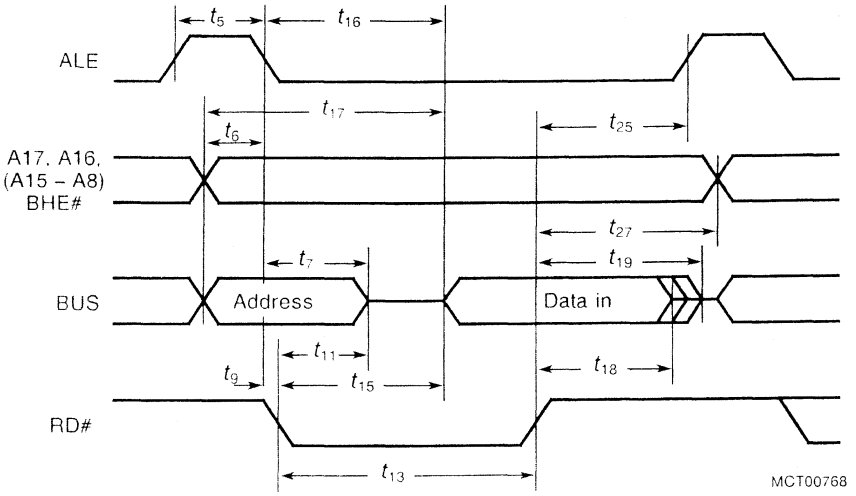
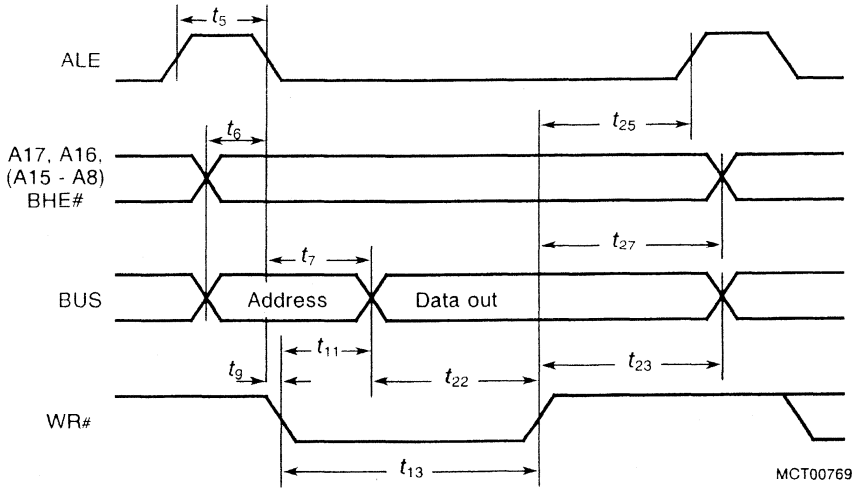


Figure 14
External Memory Write Cycle



AC Characteristics (cont'd)

Non-Multiplexed Bus with Read/Write Delay

T_A = 0 to + 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V;
C_L (for Ports 0, 1 and 4, ALE, RD#, WR#, BHE#, CLKOUT) = 100 pF
ALE cycle time = 4 TCL (150 ns at 20 MHz CPU clock)

Symbol	Parameter	CPU Clock 20 MHz		Variable Timing 1/TCL = 2 to 40 MHz		Unit
		min.	max.	min.	max.	
t_5	ALE High Time	15	–	TCL – 10	–	ns
t_6	Address Setup to ALE	10	–	TCL – 15	–	ns
t_8	ALE Falling Edge to RD#, WR#	15	–	TCL – 10	–	ns
t_{12}	RD#, WR# Low Time	40	–	2TCL – 10	–	ns
t_{14}	RD# to Valid Data In	–	35	–	2TCL – 15	ns
t_{16}	ALE Low to Valid Data In	–	60	–	3TCL – 15	ns
t_{17}	Address to Valid Data In	–	75	–	4TCL – 25	ns
t_{18}	Data Hold after RD# Rising Edge	0	–	0	–	ns
t_{20}	Data Float after RD# *)	–	35	–	2TCL – 15	ns
t_{22}	Data Valid to WR#	35	–	2TCL – 15	–	ns
t_{24}	Data Hold after WR#	15	–	TCL – 10	–	ns
t_{26}	ALE rising edge after RD#, WR#	– 10	–	– 10	–	ns
t_{28}	Address Hold after RD#, WR#	0	–	0	–	ns

*) This time may be longer if no external bus conflict can occur. For example, this requirement is always met if only code but no data are accessed externally.

Figure 15
External Memory Read Cycle

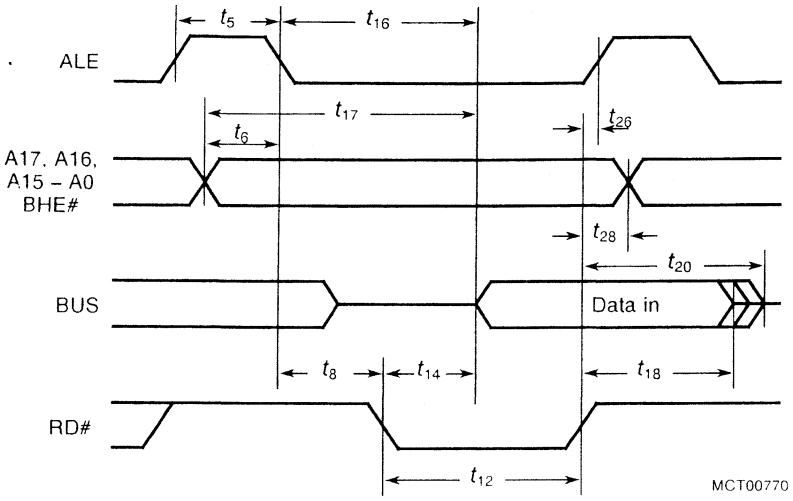
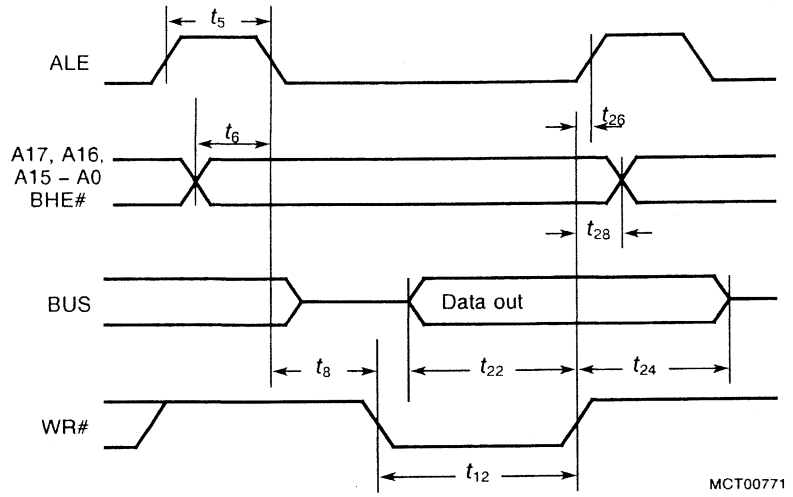


Figure 16
External Memory Write Cycle



AC Characteristics (cont'd)

Non-Multiplexed Bus without Read/Write Delay
T_A = 0 to + 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V;
C_L (for Ports 0, 1 and 4, ALE, RD#, WR#, BHE#, CLKOUT) = 100 pF
ALE cycle time = 4 TCL (100 ns at 20 MHz CPU clock)

Symbol	Parameter	CPU Clock 20 MHz		Variable Timing 1/TCL = 2 to 40 MHz		Unit
		min.	max.	min.	max.	
t_5	ALE High Time	15	–	TCL – 10	–	ns
t_6	Address Setup to ALE	10	–	TCL – 15	–	ns
t_9	ALE Falling Edge to RD#, WR#	– 10	–	– 10	–	ns
t_{13}	RD#, WR# Low Time	65	–	3TCL – 10	–	ns
t_{15}	RD# to Valid Data In	–	60	–	3TCL – 15	ns
t_{16}	ALE Low to Valid Data In	–	60	–	3TCL – 15	ns
t_{17}	Address to Valid Data In	–	75	–	4TCL – 25	ns
t_{18}	Data Hold after RD# Rising Edge	0	–	0	–	ns
t_{21}	Data Float after RD# *)	–	15	–	TCL – 10	ns
t_{22}	Data Valid to WR#	35	–	2TCL – 15	–	ns
t_{24}	Data Hold after WR#	15	–	TCL – 10	–	ns
t_{26}	ALE rising edge after RD#, WR#	– 10	–	– 10	–	ns
t_{28}	Address Hold after RD#, WR#	0	–	0	–	ns

*) This time may be longer if no external bus conflict can occur. For example, this requirement is always met if only code but no data are accessed externally.

Figure 17
External Memory Read Cycle

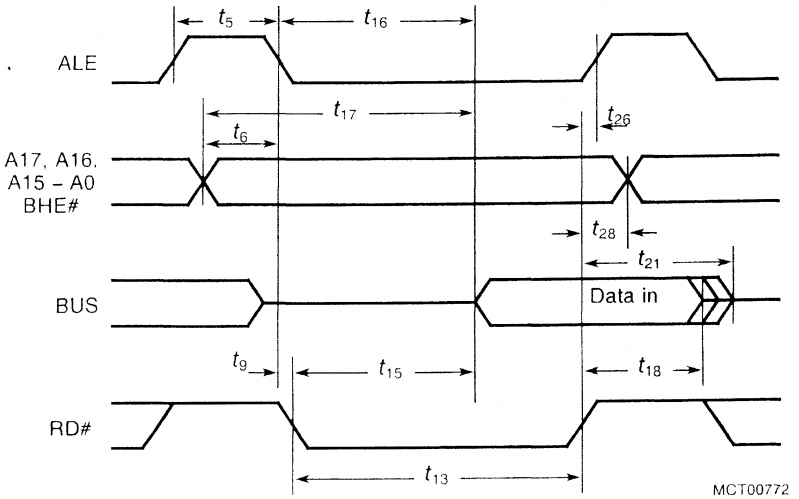
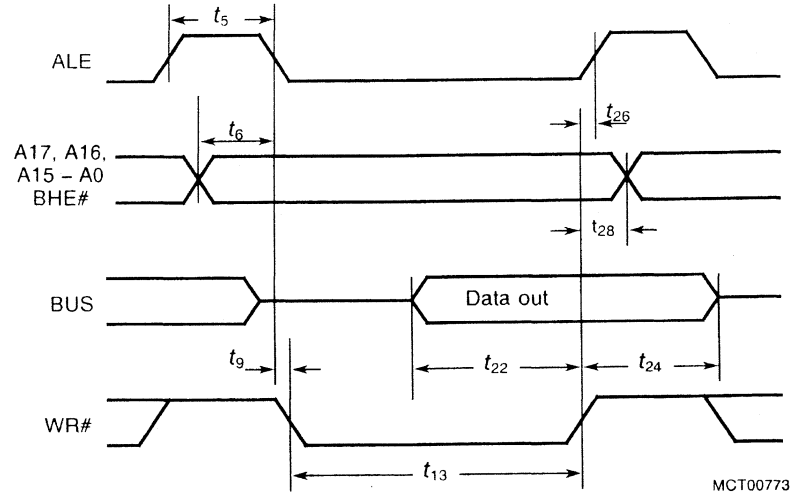


Figure 18
External Memory Write Cycle



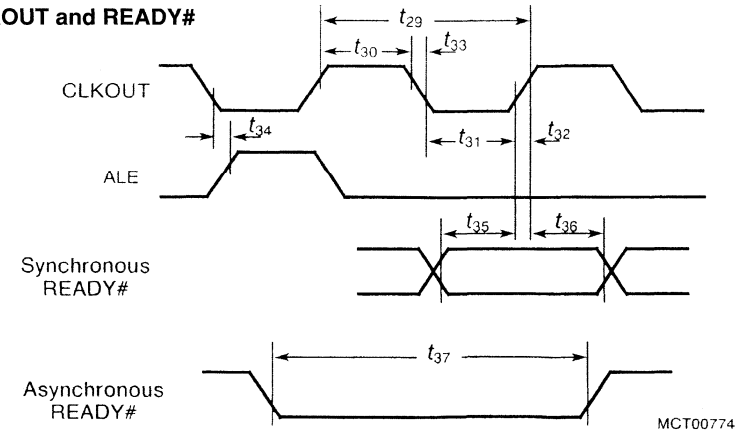
AC Characteristics (cont'd)

CLKOUT and READY#

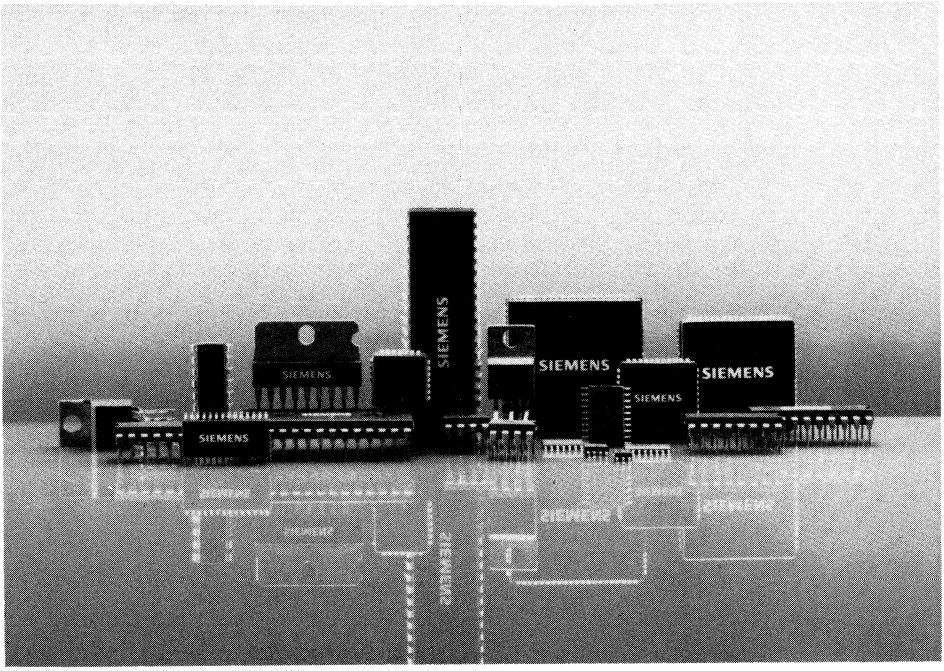
T_A = 0 to + 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V;
C_L (for Ports 0, 1 and 4, ALE, RD#, WR#, BHE#, CLKOUT) = 100 pF

Symbol	Parameter	CPU Clock 20 MHz		Variable Timing 1/TCL = 2 to 40 MHz		Unit
		min.	max.	min.	max.	
t_{29}	CLKOUT Cycle Time	50	50	2TCL	2TCL	ns
t_{30}	CLKOUT High Time	15	–	TCL – 10	–	ns
t_{31}	CLKOUT Low Time	15	–	TCL – 10	–	ns
t_{32}	CLKOUT Rise Time	–	5	–	5	ns
t_{33}	CLKOUT Fall Time	–	5	–	5	ns
t_{34}	ALE Rising to CLKOUT Falling Edge	0	10	0	10	ns
t_{35}	Synchronous READY# Setup Time to CLKOUT	10	–	10	–	ns
t_{36}	Synchronous READY# Hold Time after CLKOUT	10	–	10	–	ns
t_{37}	Asynchronous READY# Hold Time	65	–	2TCL + 15	–	ns

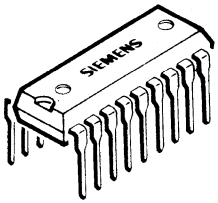
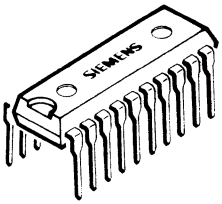
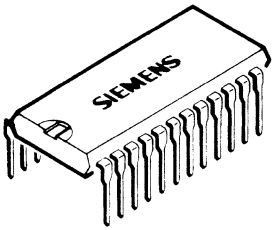
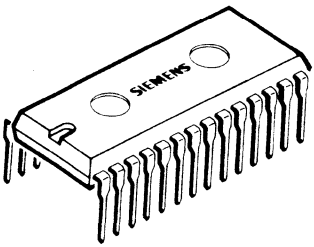
Figure 19
CLKOUT and READY#

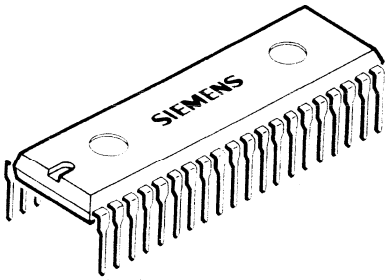


Summary of Package Outlines



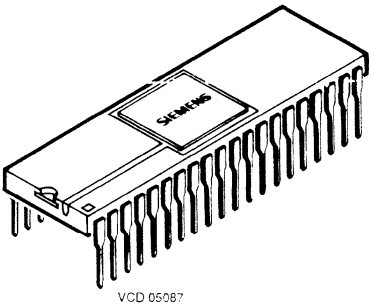
Package Outlines

 VPD 05035	**Plastic Package, P-DIP-18** (dual-in-line package) **20A18 DIN 41870 T9**
 VPD 05031	**Plastic Package, P-DIP-20** (dual-in-line package) **20A20 DIN 41870 T9**
 VRD 05034	**Plastic Package, P-DIP-24** (dual-in-line package) **20A24 DIN 41870 T10**
 VPD 05037	**Plastic Package, P-DIP-28** (dual-in-line package) **20A28 DIN 41870 T10**



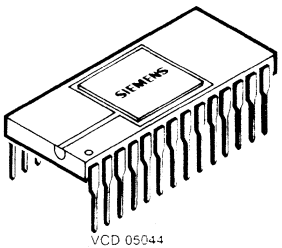
VPD 05055

Plastic Package, P-DIP-40
(dual-in-line package)
20A40 DIN 41870 T10



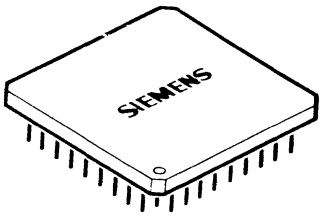
VCD 05087

Ceramic Package, C-DIP-40
(dual-in-line package)



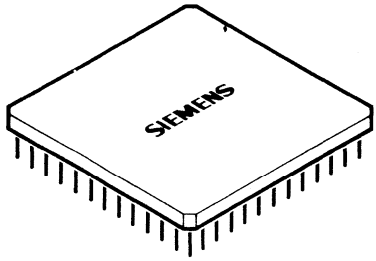
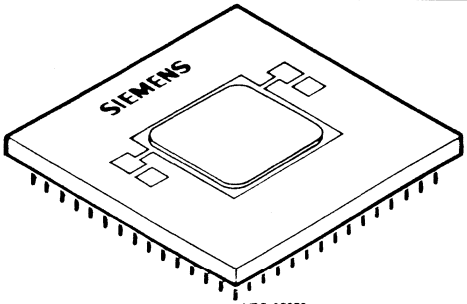
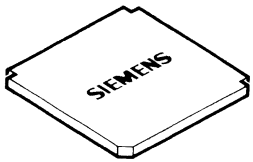
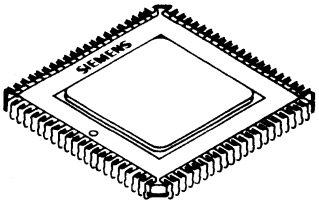
VCD 05044

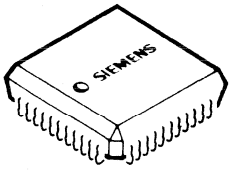
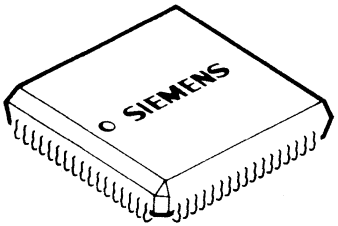
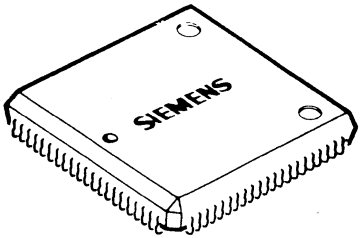
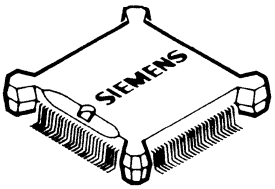
Ceramic Package,C-DIP-28
(dual-in-line package)

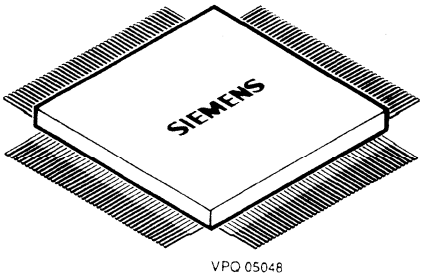


VPG 05003

Ceramic Package,C-PGA-68
(pin-grid-array)

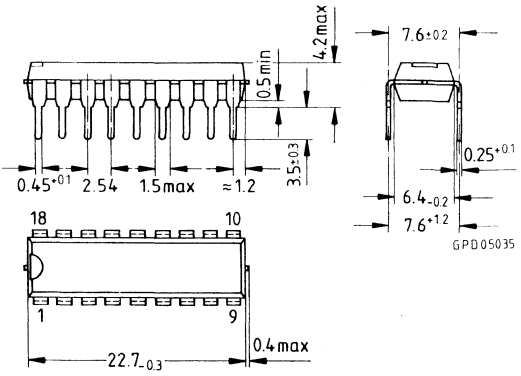
 VPL 05002	**Ceramic Package,C-PGA-88** (pin-grid-array)
 VPG 05058	**Ceramic Package,C-PGA-145** (pin-grid-array)
 VCC 05027	**Ceramic Package,C-CC-68** (chip-carrier)
 VPL 05126	**Ceramic Package,CL-CC-84** (chip-carrier)

 VPL 05102	**Plastic Package, PL-CC-44** (chip-carrier) – **SMD**
 VPL 05099	**Plastic Package, PL-CC-68** (chip-carrier) – **SMD**
 VPL 05029	**Plastic Package, PL-CC-84** (chip-carrier) – **SMD**
 VPQ 05032	**Plastic Package, P-QFP-100** (Quad-Flat-Pack) **-SMD**



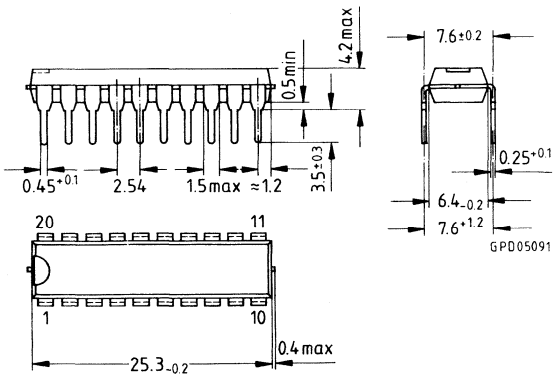
Ceramic Package,C-QFP-172
(Quad-Flat-Pack)

Plastic Package, P-DIP-18
(dual-in-line package)
20A18 DIN 41870 T9



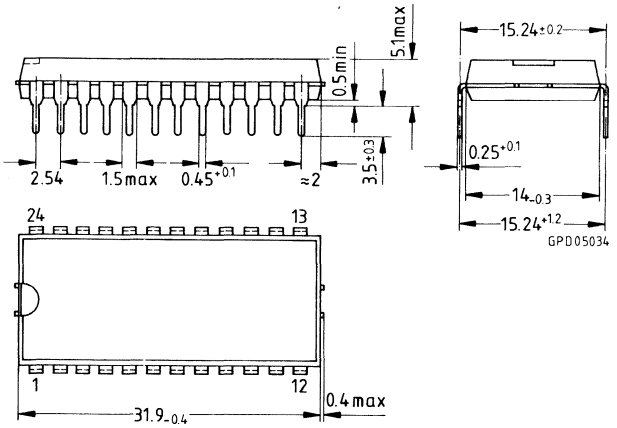
Dimensions in mm

Plastic Package, P-DIP-20
(dual-in-line package)
20A20 DIN 41870 T9



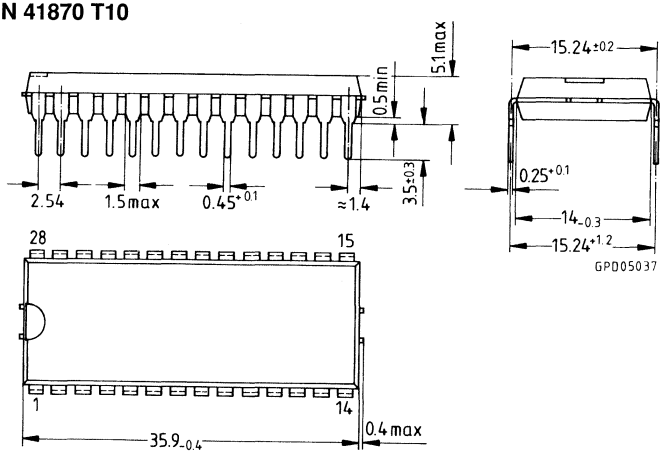
Dimensions in mm

Plastic Package, P-DIP-24
(dual-in-line package)
20A24 DIN 41870 T10



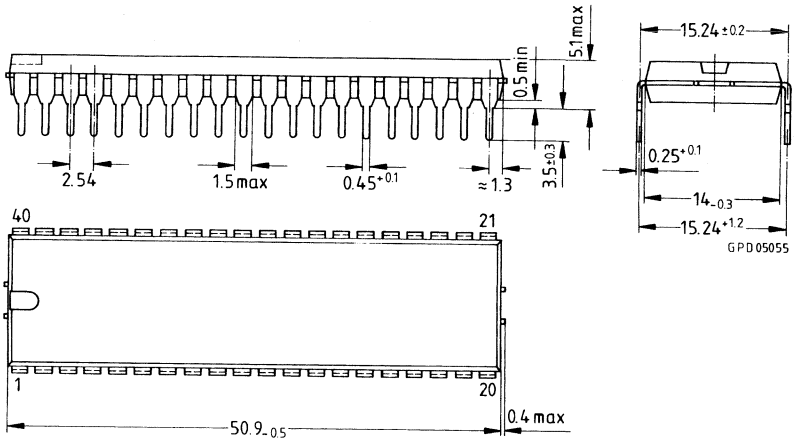
Dimensions in mm

Plastic Package, P-DIP-28
(dual-in-line package)
20A28 DIN 41870 T10



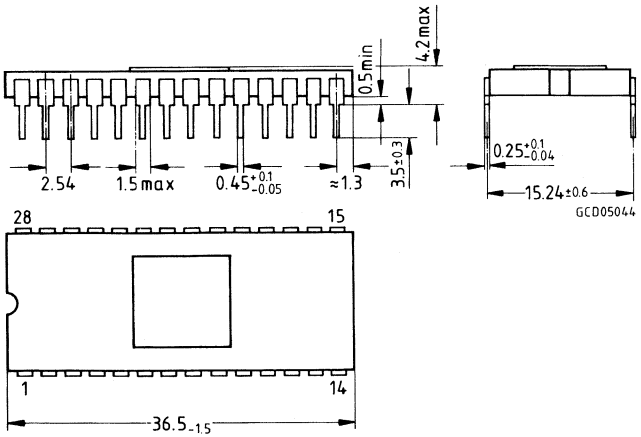
Dimensions in mm

Plastic Package, P-DIP-40
(dual-in-line package)
20A40 DIN 41870 T10



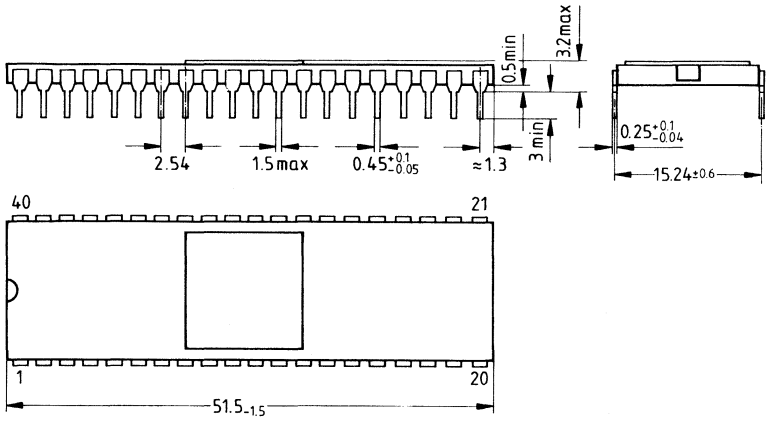
Dimensions in mm

Plastic Package, C-DIP-28
(dual-in-line package)



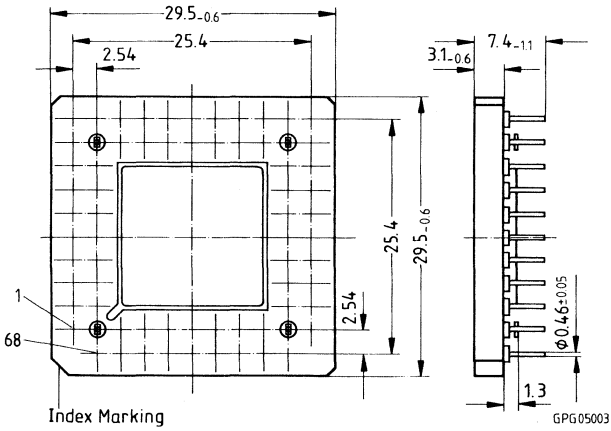
Dimensions in mm

Ceramic Package, C-DIP-40
(dual-in-line package)



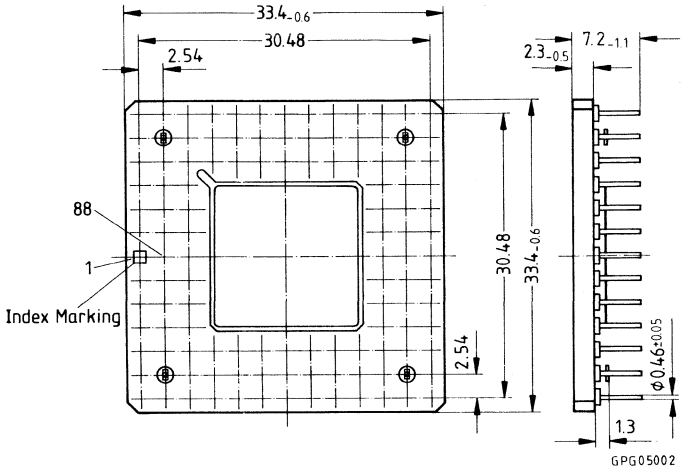
Dimensions in mm

Ceramic Package, C-PGA-68
(pin-grid-array)



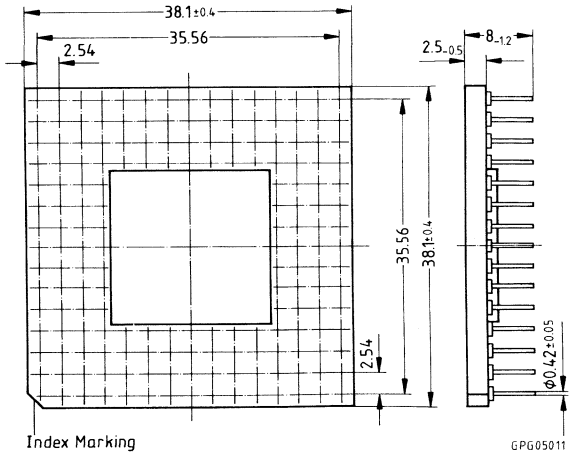
Dimensions in mm

Ceramic Package, C-PGA-88
(pin-grid-array)



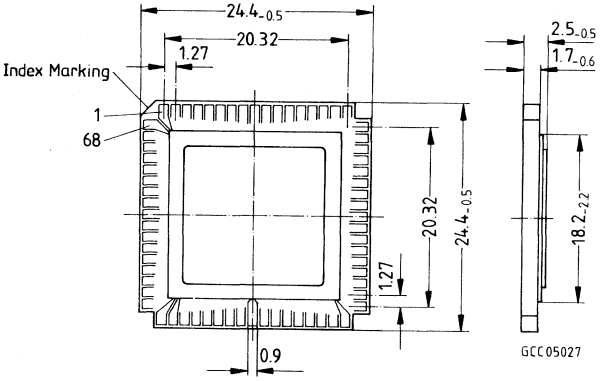
Dimensions in mm

Ceramic Package, C-PGA-145
(pin-grid-array)



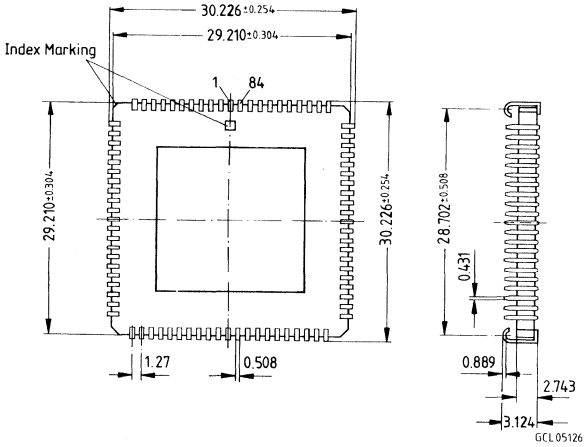
Dimensions in mm

Ceramic Package, C-CC-68
(chip-carrier)



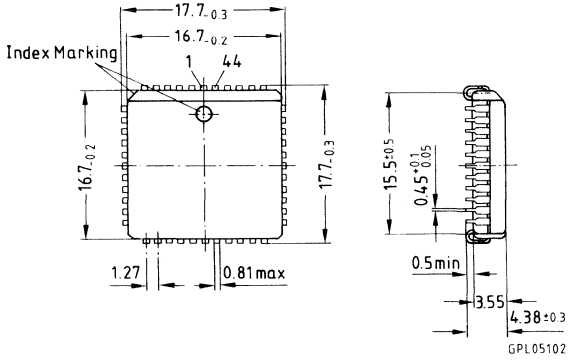
Dimensions in mm

Ceramic Package, CL-CC-84
(chip-carrier)



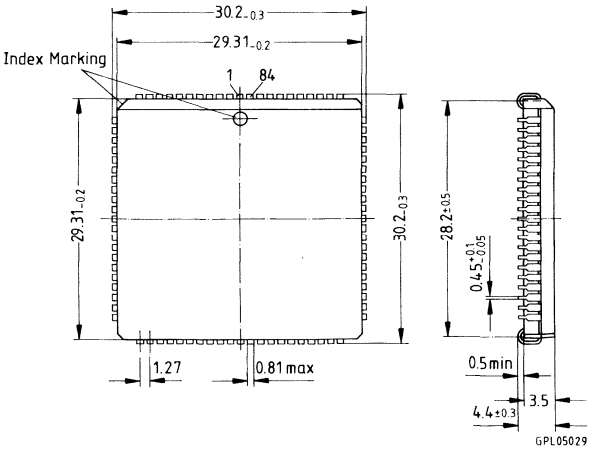
Dimensions in mm

Plastic Package, PL-CC-44
(chip-carrier) – **SMD**



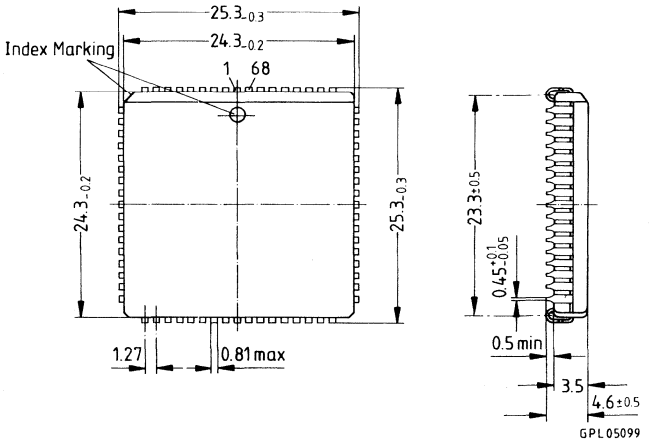
Dimensions in mm

Plastic Package, PL-CC-84
(chip-carrier) – **SMD**



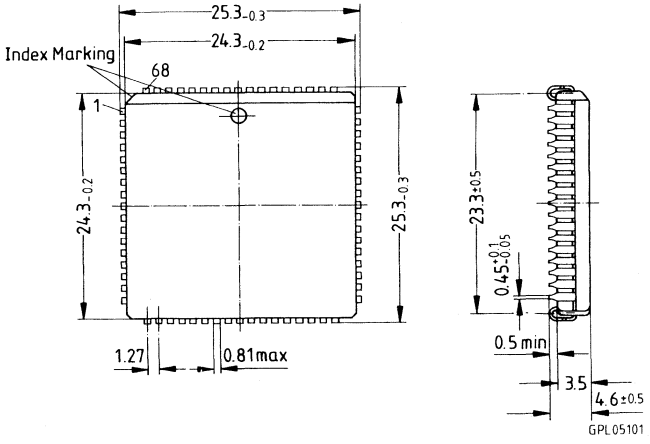
Dimensions in mm

Plastic Package, PL-CC-68
(chip-carrier) – **SMD**



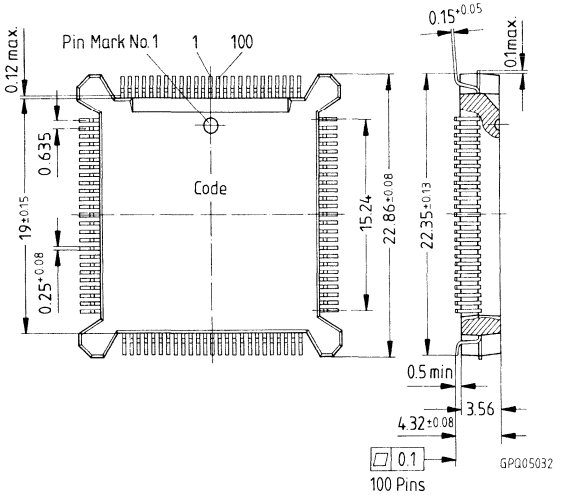
Dimensions in mm

Plastic Package, PL-CC-68
(chip-carrier) – **SMD**



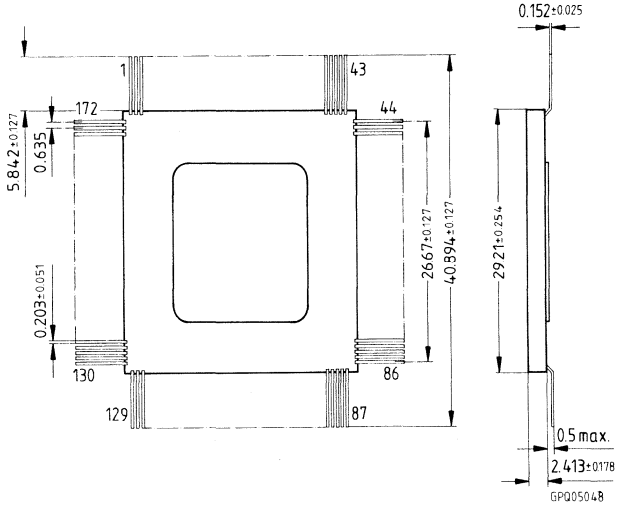
Dimensions in mm

Plastic Package, P-QFP -100
(Quad-Flat-Pack) **- SMD**



Dimensions in mm

Ceramic Package, C-QFP -172
(Quad-Flat-Pack)



Dimensions in mm

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9/90a

Literaturhinweis
Information on Literature

Titel/Title	Bestell-Nr./Ordering No.	DM
Datenkataloge / Data Catalogs		
Microcontrollers	B158-B6213-X-X-7600	20,-
Microprocessors and Support Components	B158-B6256-X-X-7600	20,-
PC Peripherals and System Components	B158-B6255-X-X-7600	20,-
Memory Components	B166-B6290-X-X-7600	15,-
Benutzer-Handbücher / User's Manuals		
SAB 80512/80532, 8-bit Microcontroller	B2-B3808-X-X-7600	15,-
SAB 80515/80535 – SAB 80C515/80C535 (CMOS), 8-bit Microcontroller	B158 H6367-X-X-7600	15,-
SAB 80C517/80C537, CMOS, 8-bit Microcontroller	B258-B6075-X-X-7600	15,-
SAB 80C166/83C166 – 16-bit CMOS Single-Chip Microcontroller	B158-B6247-X-X-7600	20,-
Addendum to User's Manual SAB 80C166/83C166	B158-H6345-X-X-7600	–
SAB 8256A – MUART, Programmierbarer Multifunktionsbaustein	B2-B2494	10,-
SAB 8256A – UART, Programmable Multifunction Controller	B2-B2494-X-X-7600	10,-
SAB 82257 – High Performance DMA Controller for 16-bit Microcomputer Systems	B2-B3486-X-X-7600	15,-
SAB 82258A/SAB 82C258A – ADMA, Advanced DMA Controller for 16-/32-bit Microcomputer Systems	B158-B6305-X-X-7600	15,-
Produktschriften / Product Information		
SAB 80512 – Ein-Chip Mikrocontroller	B2-B3693	–
SAB 80512 – Single-Chip Microcontroller	B2-B3693-X-X-7600	–
SAB 80515 – Ein-Chip Mikrocontroller	B2-B3340	–
SAB 80515 – Single-Chip Microcontroller	B2-B3340-X-X-7600	–
SAB 8051x – 8-bit Mikrocontroller-Familie mit den neuesten Familienmitgliedern SAB 80C515, 80C517	B258-B6150	–
The SAB 8051x – 8-bit Microcontroller Family with its new Members SAB 80C515, 80C517	B258-B6150-X-X-7600	–
SAB 80C166/83C166 High-Performance16-bit CMOS Single-Chip Microcontroller	B158-B6227-X-X-7600	–
SAB 82258A/SAB 82C258A – ADMA Advanced DMA Controller for 16-/32-bit Microcomputer Systems	B158-B6274-X-X-7600	–
SAB 82511 – TBM, Token Bus Modem	B2-B3796-X-X-7600	–
Multifunktionscontroller (SAB 82556) für serielle Schnittstellen	B258-B6166	–
Themenschriften / Special-Subject Brochures		
Der Mega-Chip	B9-B3971	–
The Mega-Chip	B9-B3971-X-X-7600	–
MEGA Perfektion – Qualität in Siemens 1-Mbit DRAMs	B166-B6286-V1	–
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